Compal Confidential

QAQ10/11

LA-8581P REV0.1 Schematic

Intel Ivy Bridge/Pather Point

UMA&OPT

2011-09-28 Rev 0.1

Security Classification	Compal Secret Data		
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Title: Cover Page

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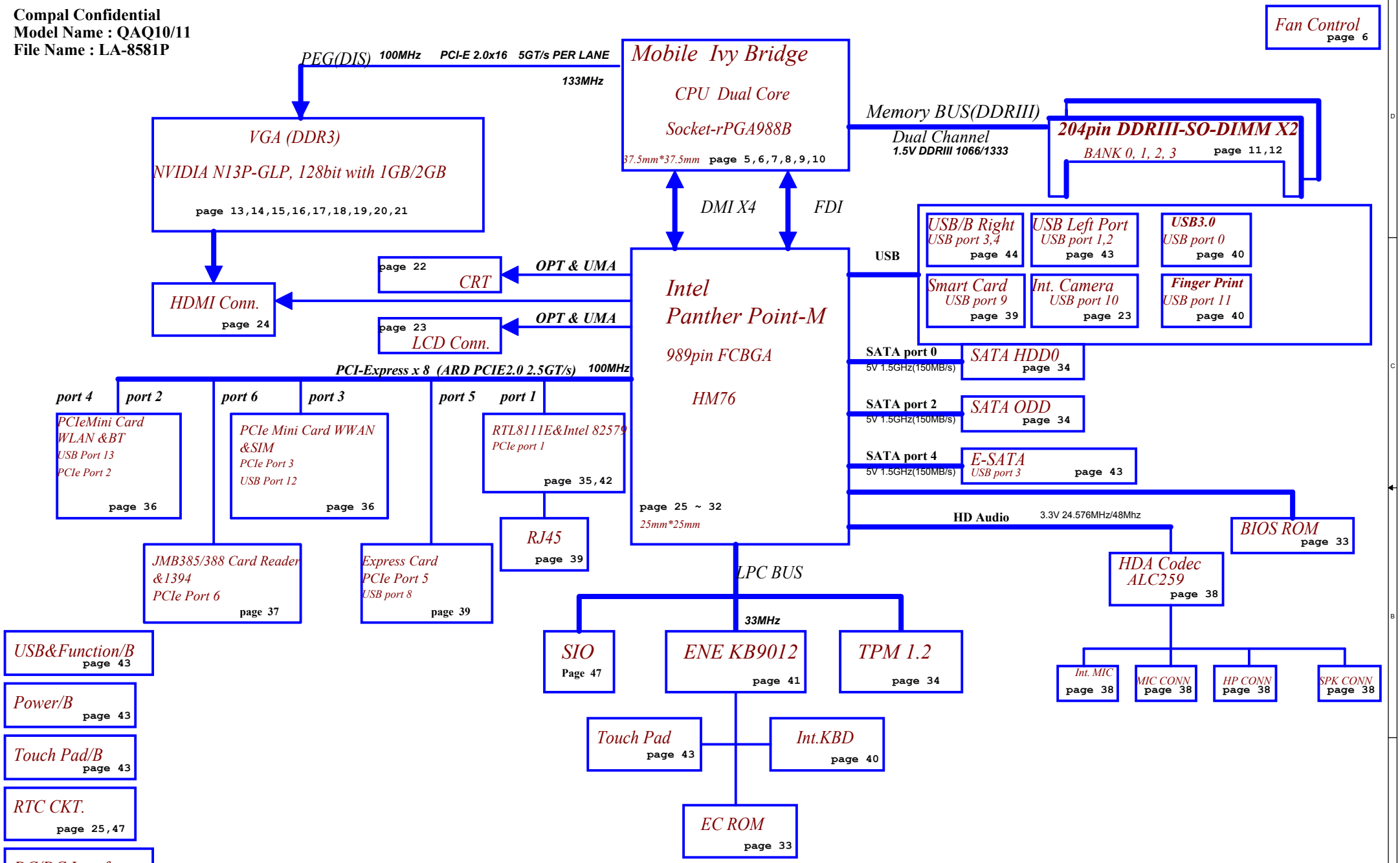
Model Name : QAQ10/11
File Name : LA-8581P



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Title	Block Diagrams	
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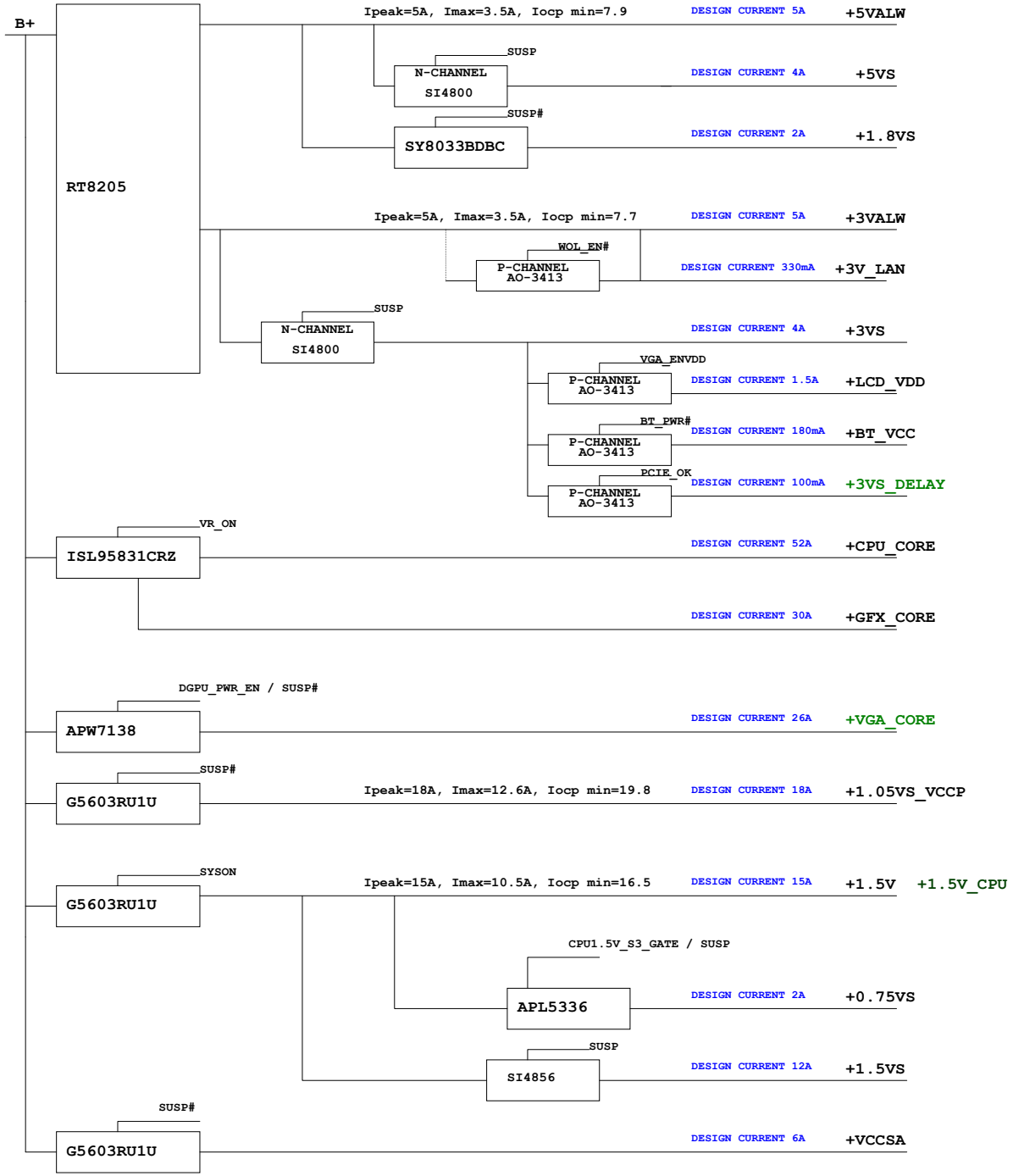

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Title: Power Map

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB930	
+3VL	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB930	
+3VS	GPU Thermal Sensor	
+3VALW	PCH	

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Slot#1--WLAN	

BOM configu table

SKU	Description	Bom config	
1	QAQ00 UMA GIGA W/HDMI	DA8@/8111E@/PCH@/UMA@/385@/IN_TPM@ TPM@/SM@/USB30@	4619F230L01
2	QAQ01 DIS DU N12GE2G W/HDMI	DA8@/8111E@/PCH@/OPT@/388@/USB20@/12GE@	4619F230L11
3	QAQ02 UMA VPRO W/HDMI	DA8@/VPRO@/385@/USB20@/TPM@/IN_TPM@/SM@	4619F230L21
4			
5			
6			
7			
8			

DA8@/8111E@/PCH@/UMA@/385@/IN_TPM@/TPM@/SM@/USB30@/OPT@/388@/USB20@/VPRO@/WB_TPM@

X76 AND VGA configu table

SKU	Description	Config	
1	4619F230L11	ZZZ SAM1G8@ SAM 1G; ZZZ HY1G8@ Hynix 1G; UV1 12GE@ N12P-GE	QAQ01 DIS DU N12GE2G W/HDMI
2		ZZZ SAM1G8@ SAM 1G; ZZZ HY1G8@ Hynix 1G; UV1 12GV2@ N12P-GV2	
3		ZZZ SAM2G@ SAM 2G; ZZZ HY2G@ Hynix 2G; UV1 12GE@ N12P-GE	
4			
5			
6			
7			

Board ID Table

Board ID	Rb / Rd / Rf	Ra/Rc/Re	VCC	V min	Vtyp	Vmax	PCB Revision
0	0	100K +/- 5%	3.3V +/- 5%	0V	0V	0V	0.1
1	8.2K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.436 V	0.503 V	0.538 V	0.3
3	33K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.712 V	0.819 V	0.875 V	0.4
4	56K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.036 V	1.185 V	1.264 V	1.0
5	100K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.453 V	1.650 V	1.759 V	VPRO
6	200K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	100K +/- 5%	3.3V +/- 5%	2.500 V	3.300 V	3.300 V	

PCH And PCBA table

PCH	UPCH1 BD82HM65 SLH9D B2 FCBGA 989P PCH PCH@	UPCH1 BD82QM67 SLJ4M B3 FCBGA 989P PCH VPRO@
PCB		ZZZ DA8@ PCB LA-7661P REV01

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Title: Notes List

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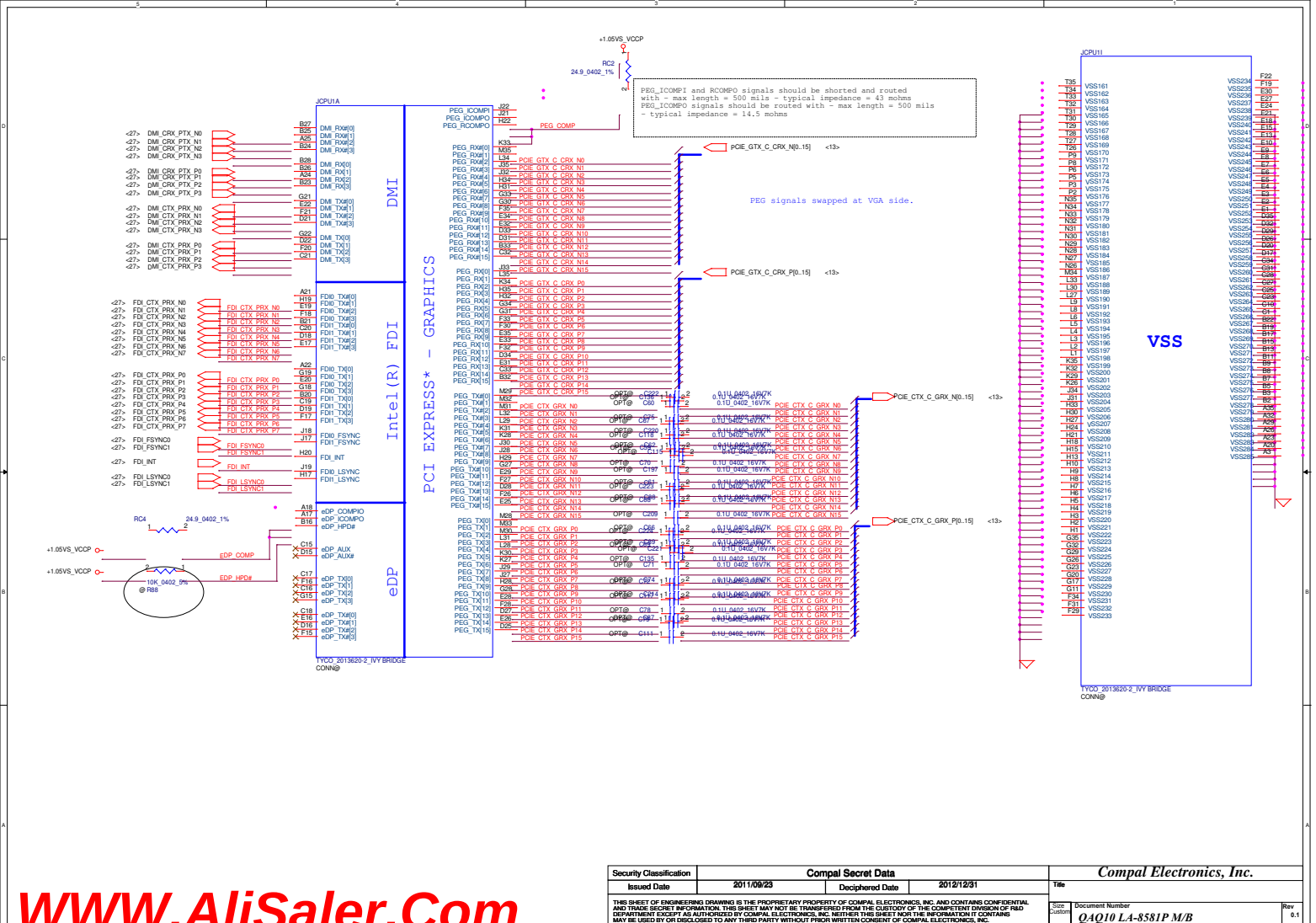

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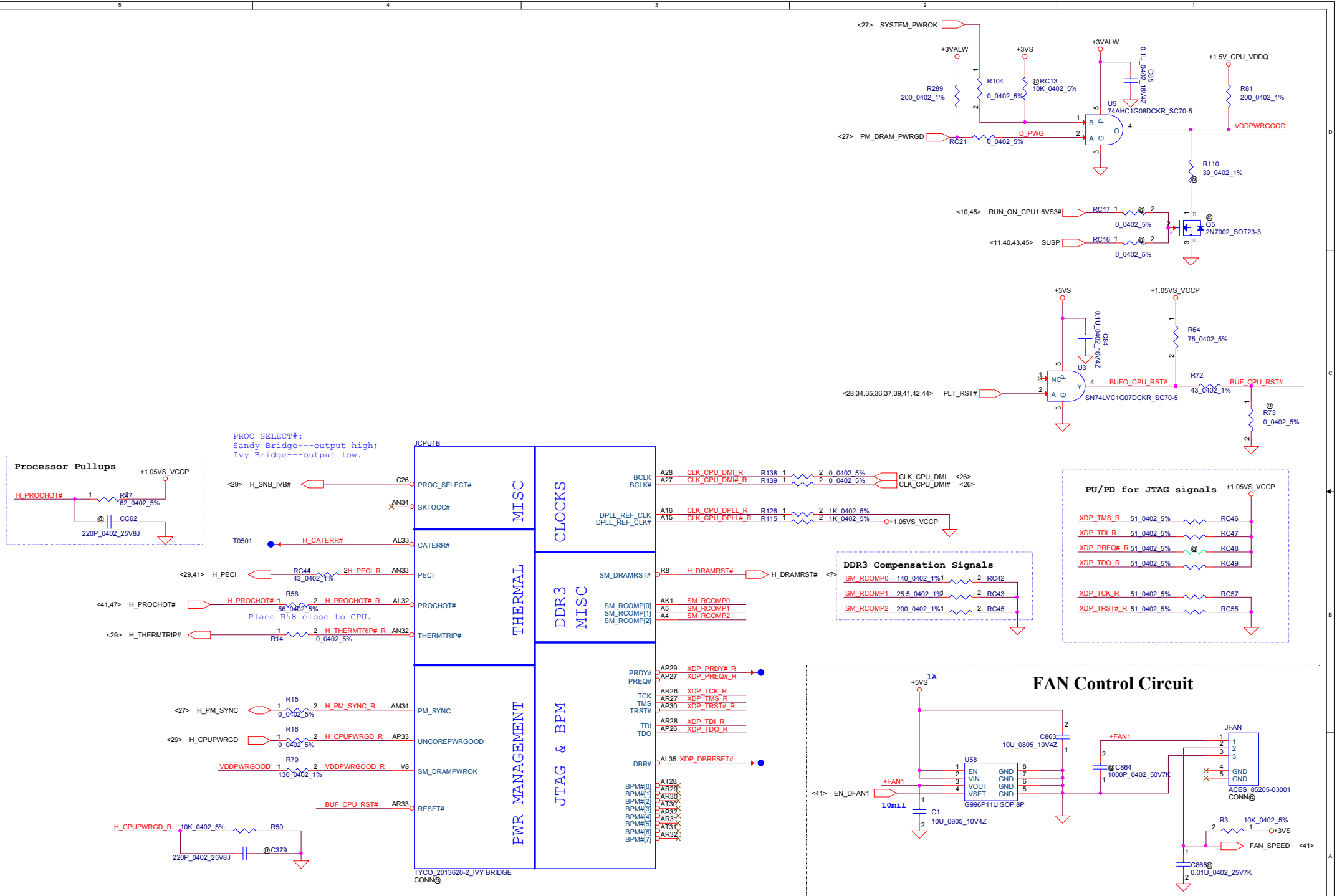

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Compal Electronics, Inc.
Title: PROCESSOR(2/6) PM,XDP,CLK
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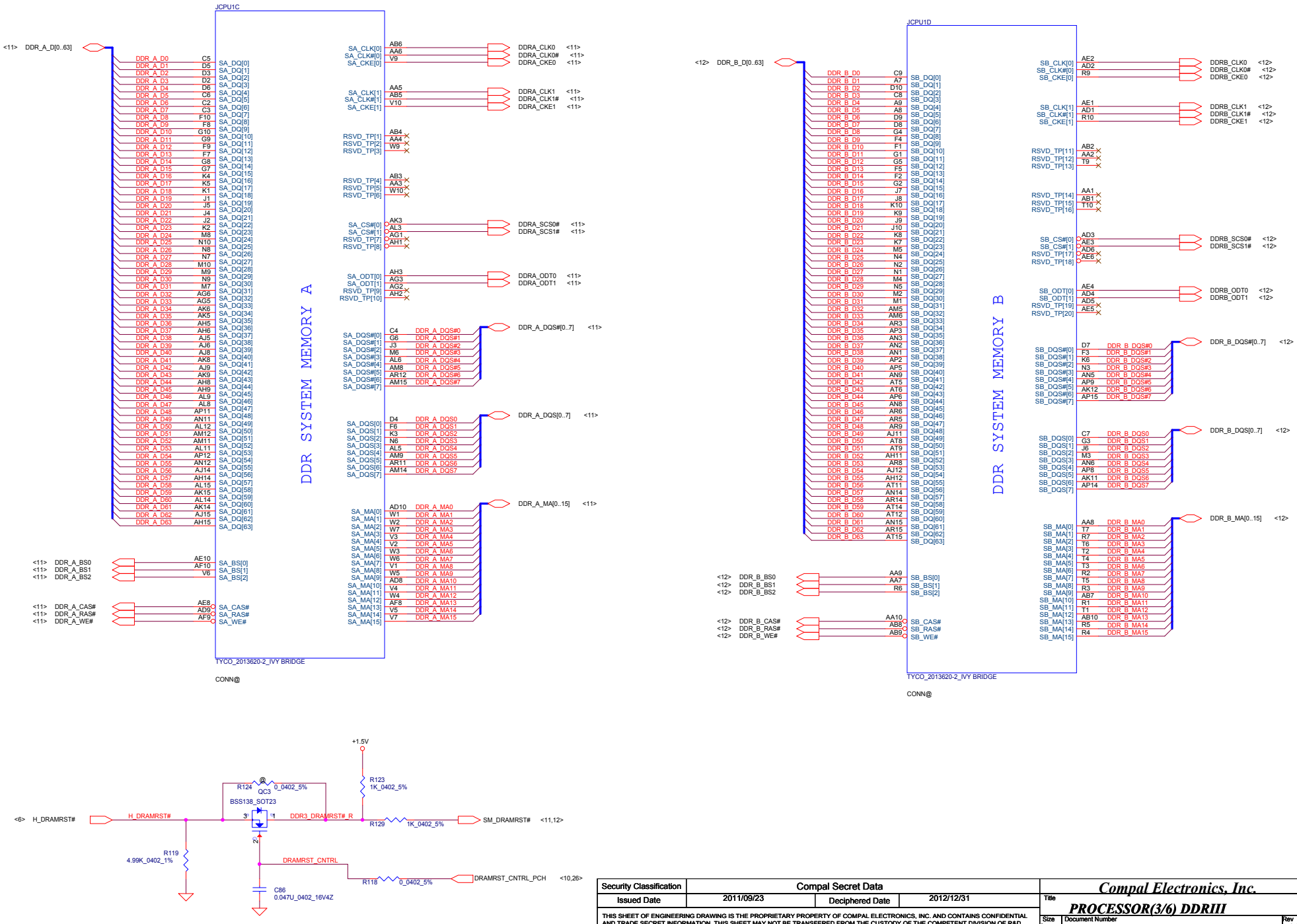

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Title: PROCESSOR(3/6) DDRIII

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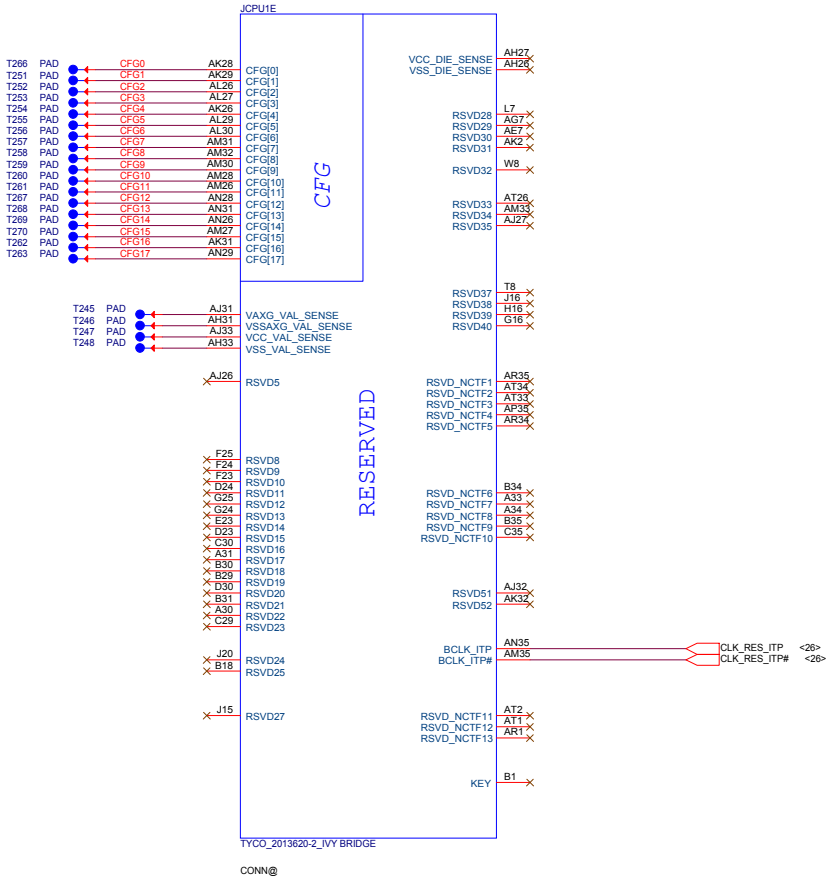
CFG[1:0]: reserved configuration lane.

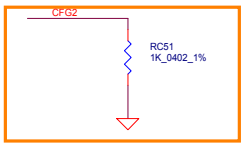
CFG[3]: reserved

CFG[17:7]: reserved configuration lanes.

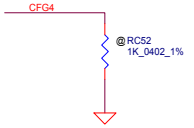
CFG[17:0]:
Processor internal pull up 5~15Kohm to VCCIO



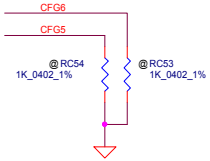
CFG Straps for Processor



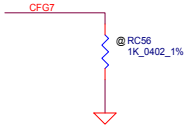
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/6) RSVD,CFG

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POWER

JCPU1H

VSS

TYCO_2013620-2_IVY BRIDGE

CONN@

JCPU1F

+VCC_CORE

97A

+1.05VS_VCCP

8.5A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

Package Sensing Recommendations--PDDG P30

Sense	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	25.5-34.5ohm	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE		
VCCIO_SENSE / VSS_SENSE_VCCIO	55ohm	
VCCSA		

Place the PU resistors RC60, RC137 close to CPU.

Place the PU resistors R53, R54 close to CPU

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Title: PROCESSOR(5/6) PWR,BYPASS

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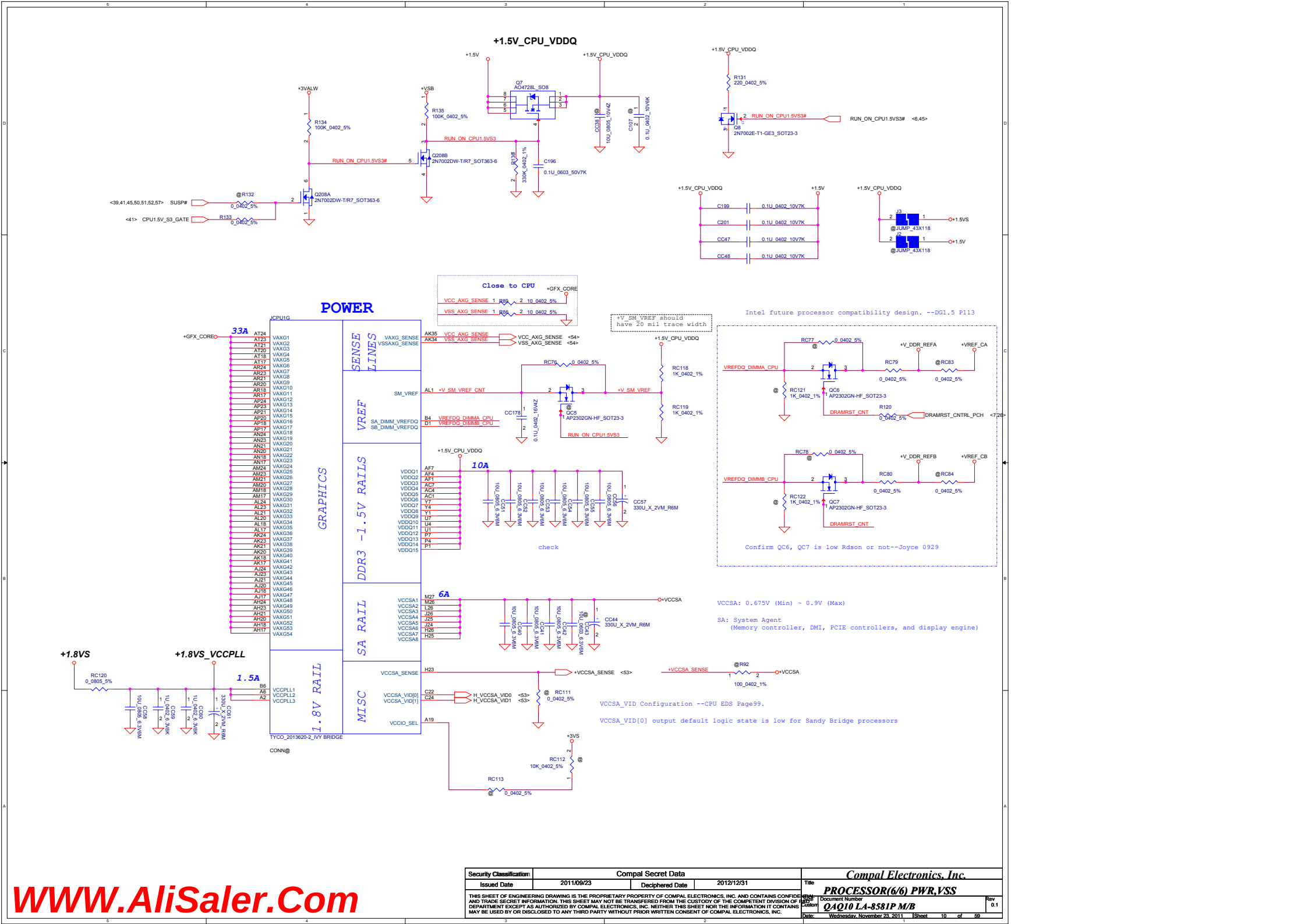

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Title: PROCESSOR(6/6) PWR,VSS

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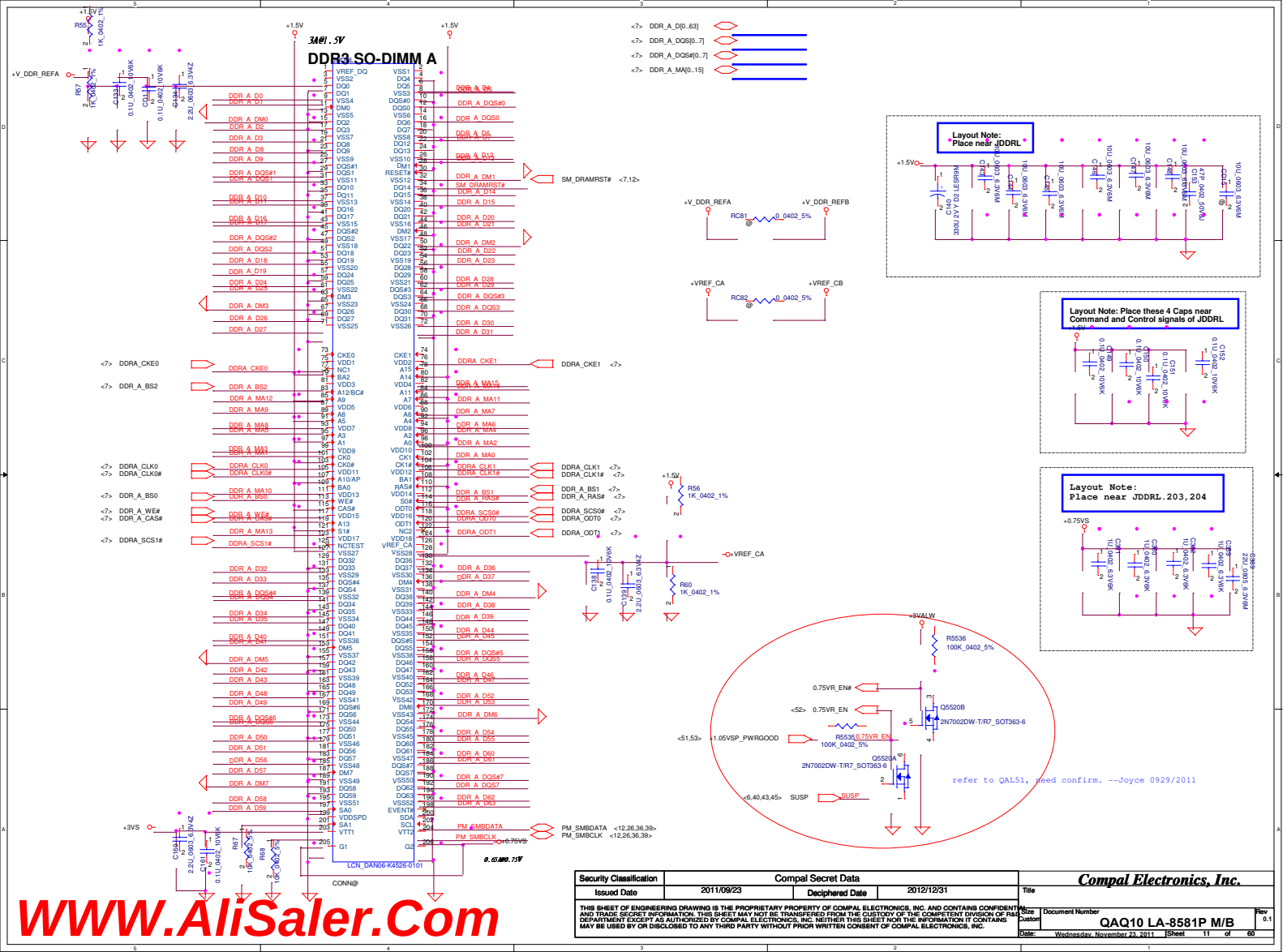

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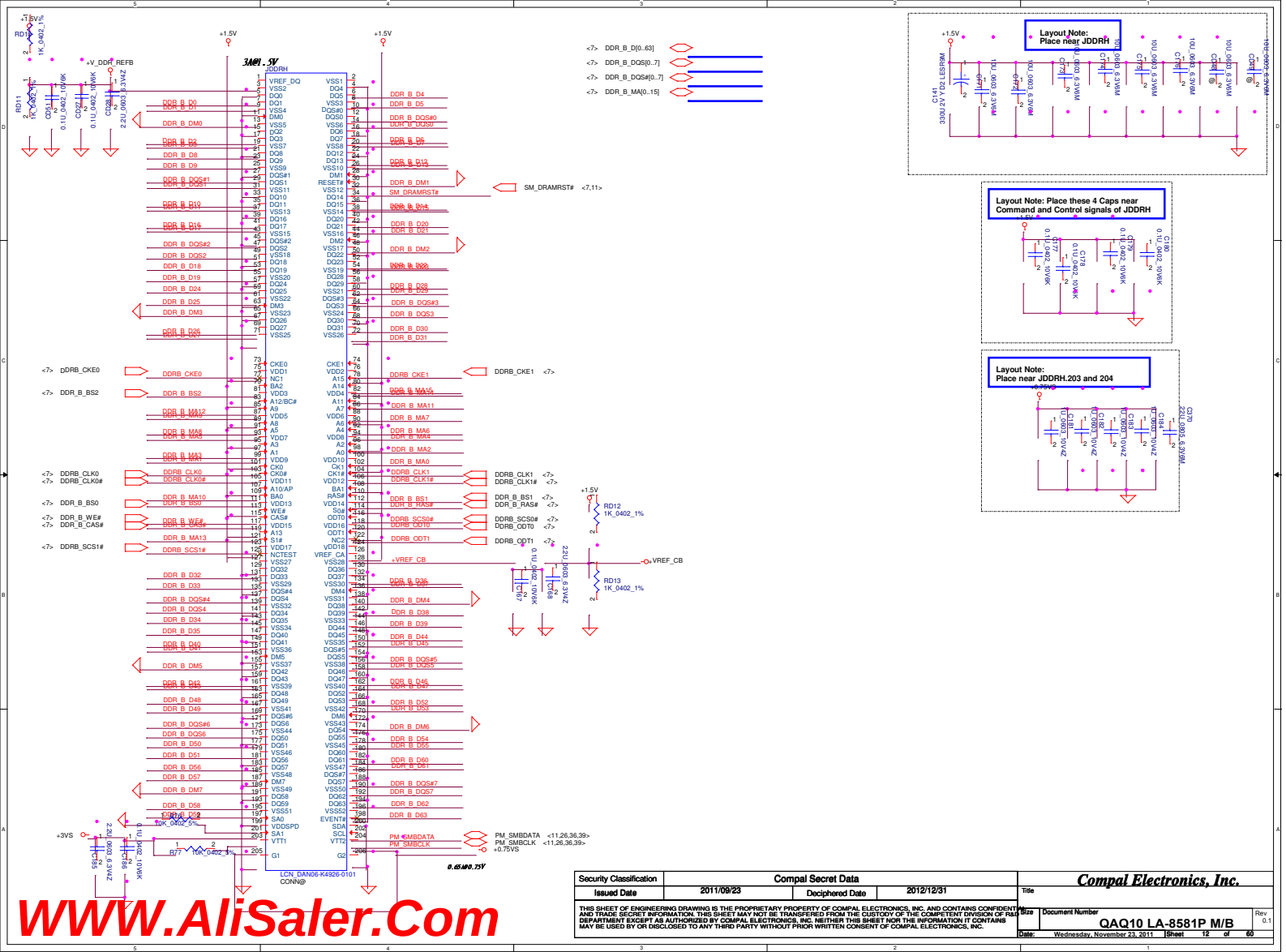

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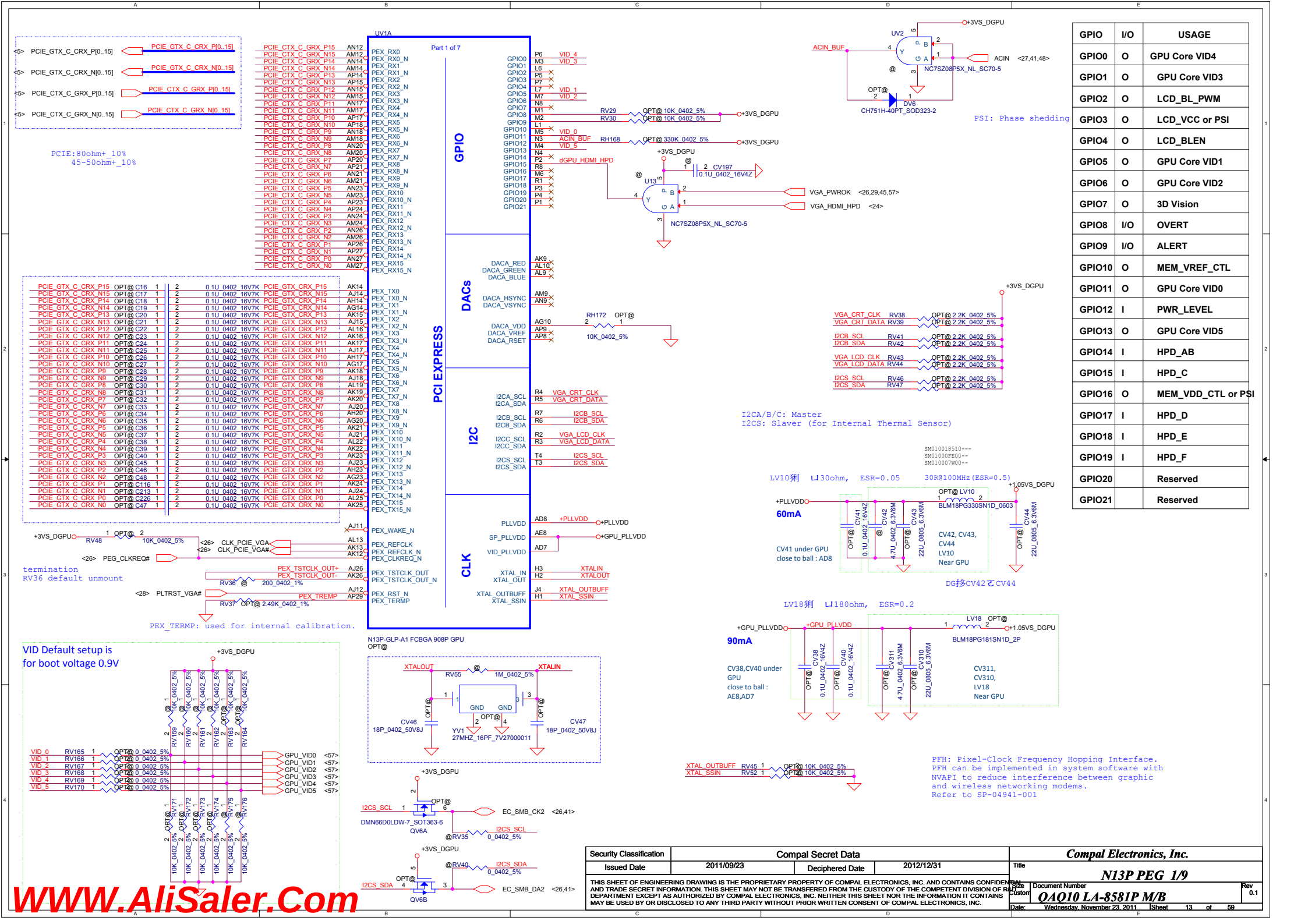

GPIO	I/O	USAGE
GPIO0	O	GPU Core VID4
GPIO1	O	GPU Core VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC or PSI
GPIO4	O	LCD_BLEN
GPIO5	O	GPU Core VID1
GPIO6	O	GPU Core VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU Core VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU Core VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL or PSI
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

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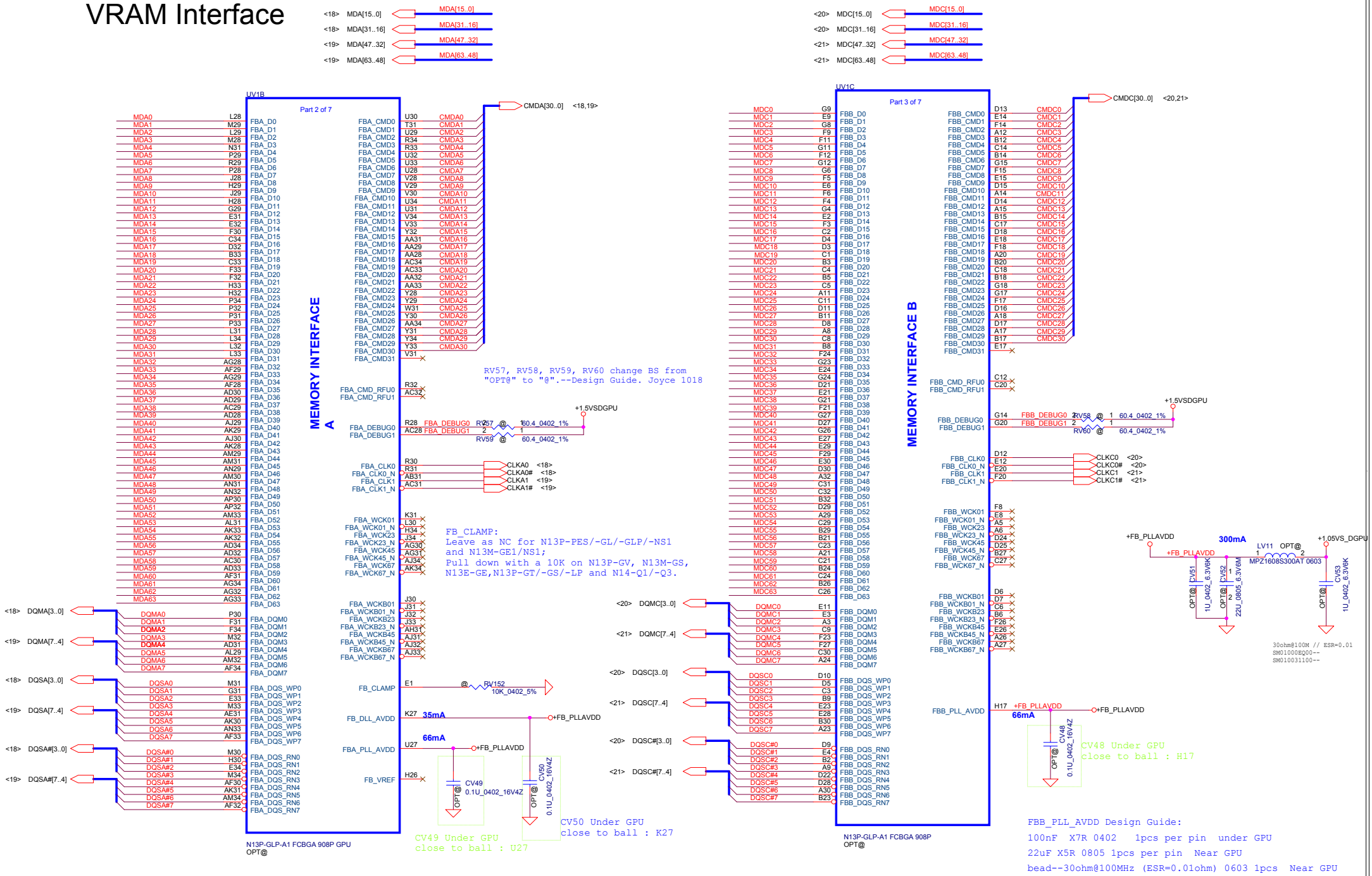
VRAM Interface



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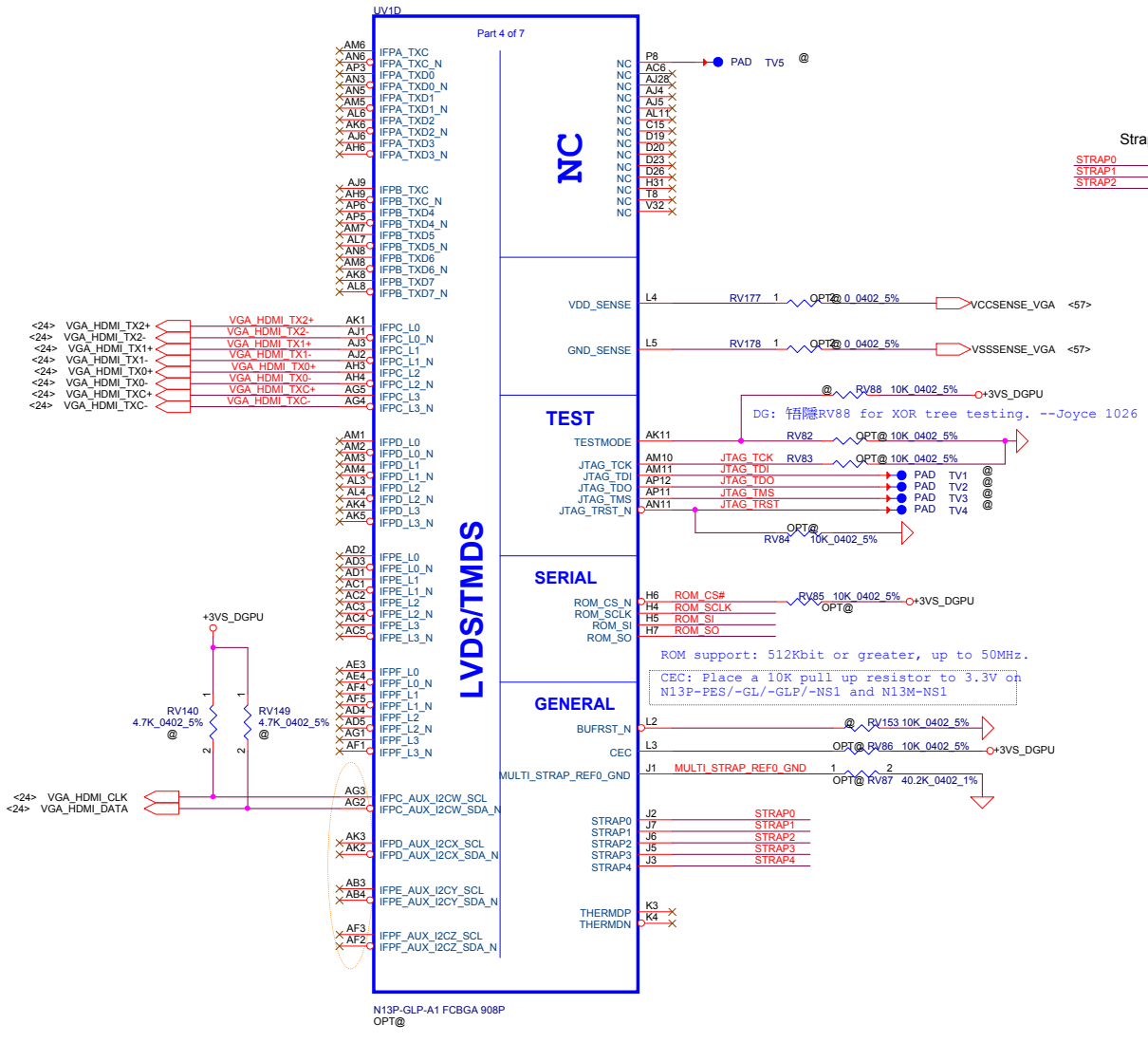
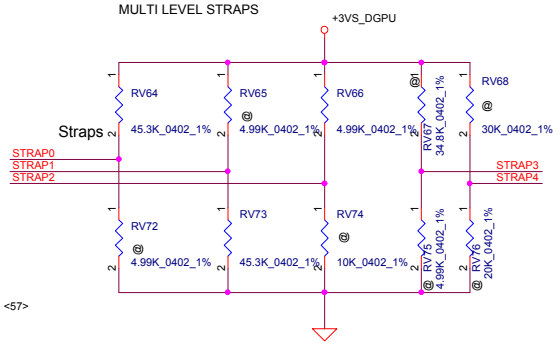
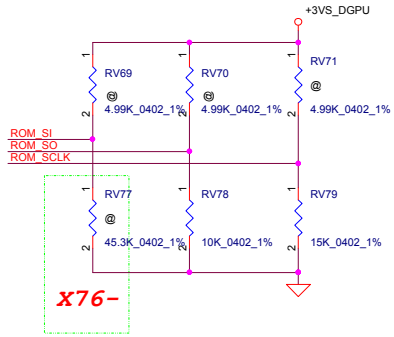
Title: N13P VRAM 2/9			
Size: Custom	Document Number: QAQ10 LA-8581P M/B		Rev: 0.1
Date: Wednesday, November 23, 2011	Sheet 14 of 59		







Physical strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB [1]	FB [0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER [3]	USER [2]	USER [1]	USER [0]
STRAP1	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	PCI-DEVID [3]	PCI-DEVID [2]	PCI-DEVID [1]	PCI-DEVID [0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull up to 3V	Pull down to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR
0 No VBIOS ROM
1 BIOS ROM is present (Default)

PEX_PLL_EN_TERM: PLL termination setting
0 Disable (Default)
1 Enable

PCIE_MAX_SPEED
0 Limited to PCIE GEN 1
1 PCIE GEN 2/3 capable

FB [1:0]: N13x FB Aperture Size
0 RESERVED
1 RESERVED
2 256 MB (Default)
3 RESERVED

USER Straps
1111 EDID is used
others: DG-05587 Page195

3GIO_PAD_CFG
0000--0101 RESERVED
0110 Notebook (default)
0111--1111 RESERVED

For N13P-GLP strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GLP	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 15K	RV70 PD 30K	RV71 PD 15K
	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 20K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 35K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 45K	RV70 PD 30K	RV71 PD 15K

For N13P-PES :
Strap 0 : PU45
Strap 1 : PD35
Strap 2 : PU35
ROM_SCLK : PU15
ROM_SI : PD35
ROM_SO : PD10

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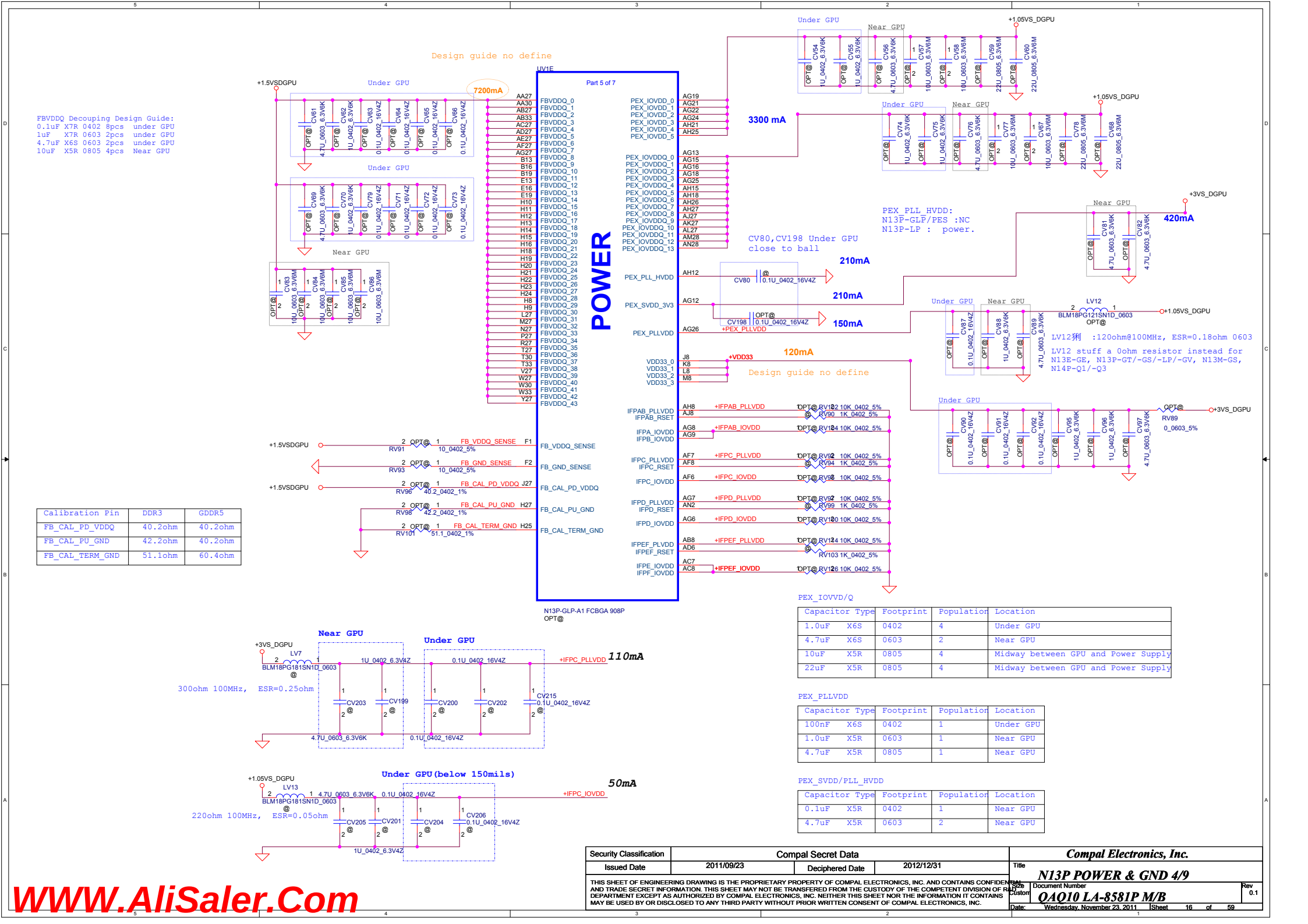
Compal Electronics, Inc.

Title: N13P LVDS 3/9

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

Date: Wednesday, November 23, 2011 | Sheet 15 of 59



Calibration Pin	DDR3	GDDR5
FB_CAL_PD_VDDQ	40.2ohm	40.2ohm
FB_CAL_PU_GND	42.2ohm	40.2ohm
FB_CAL_TERM_GND	51.1ohm	60.4ohm

PEX_IOVVD/Q

Capacitor Type	Footprint	Population	Location
1.0uF X6S	0402	4	Under GPU
4.7uF X6S	0603	2	Near GPU
10uF X5R	0805	4	Midway between GPU and Power Supply
22uF X5R	0805	4	Midway between GPU and Power Supply

PEX_PLLVDD

Capacitor Type	Footprint	Population	Location
100nF X6S	0402	1	Under GPU
1.0uF X5R	0603	1	Near GPU
4.7uF X5R	0805	1	Near GPU

PEX_SVDD/PLL_HVDD

Capacitor Type	Footprint	Population	Location
0.1uF X5R	0402	1	Near GPU
4.7uF X5R	0603	2	Near GPU

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Title: N13P POWER & GND 4/9

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Date: Wednesday, November 23, 2011 | Sheet 16 of 59

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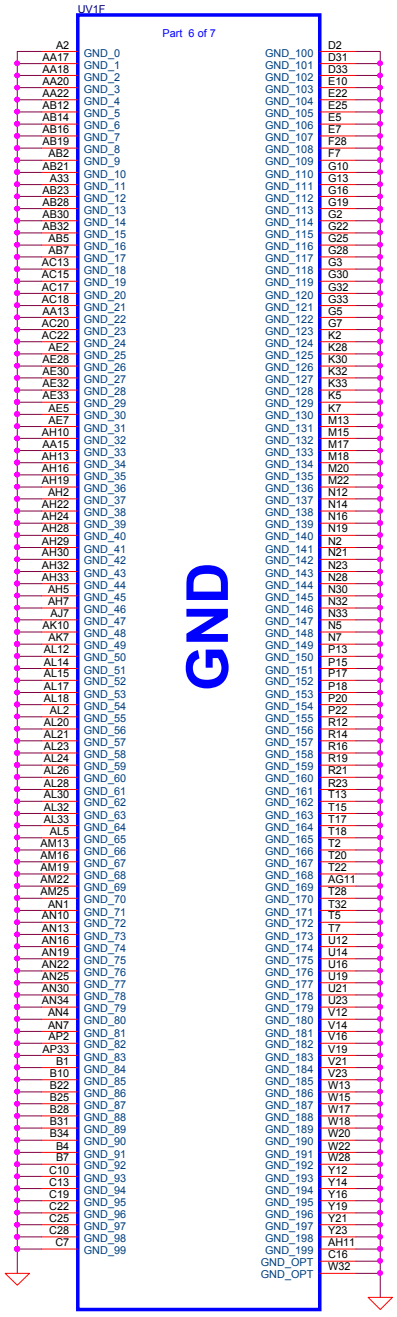

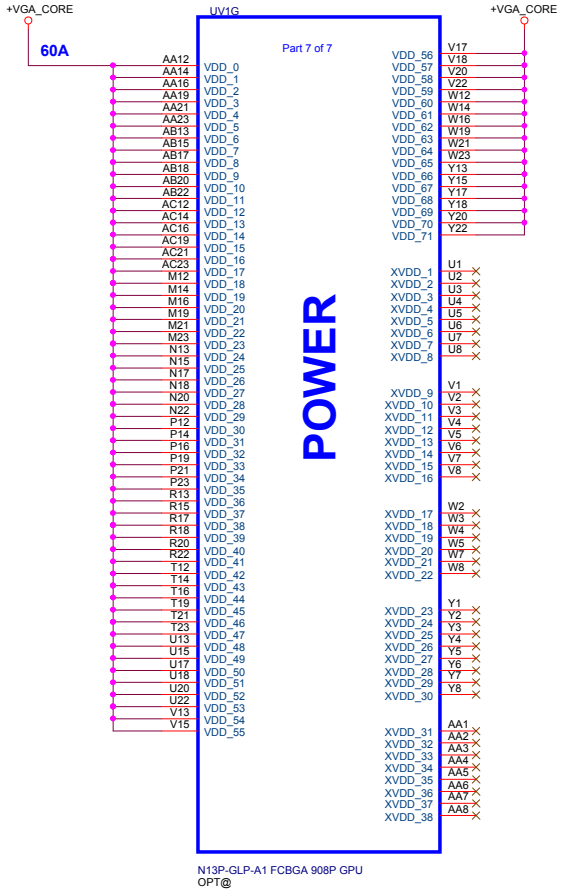

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Compal Electronics, Inc.

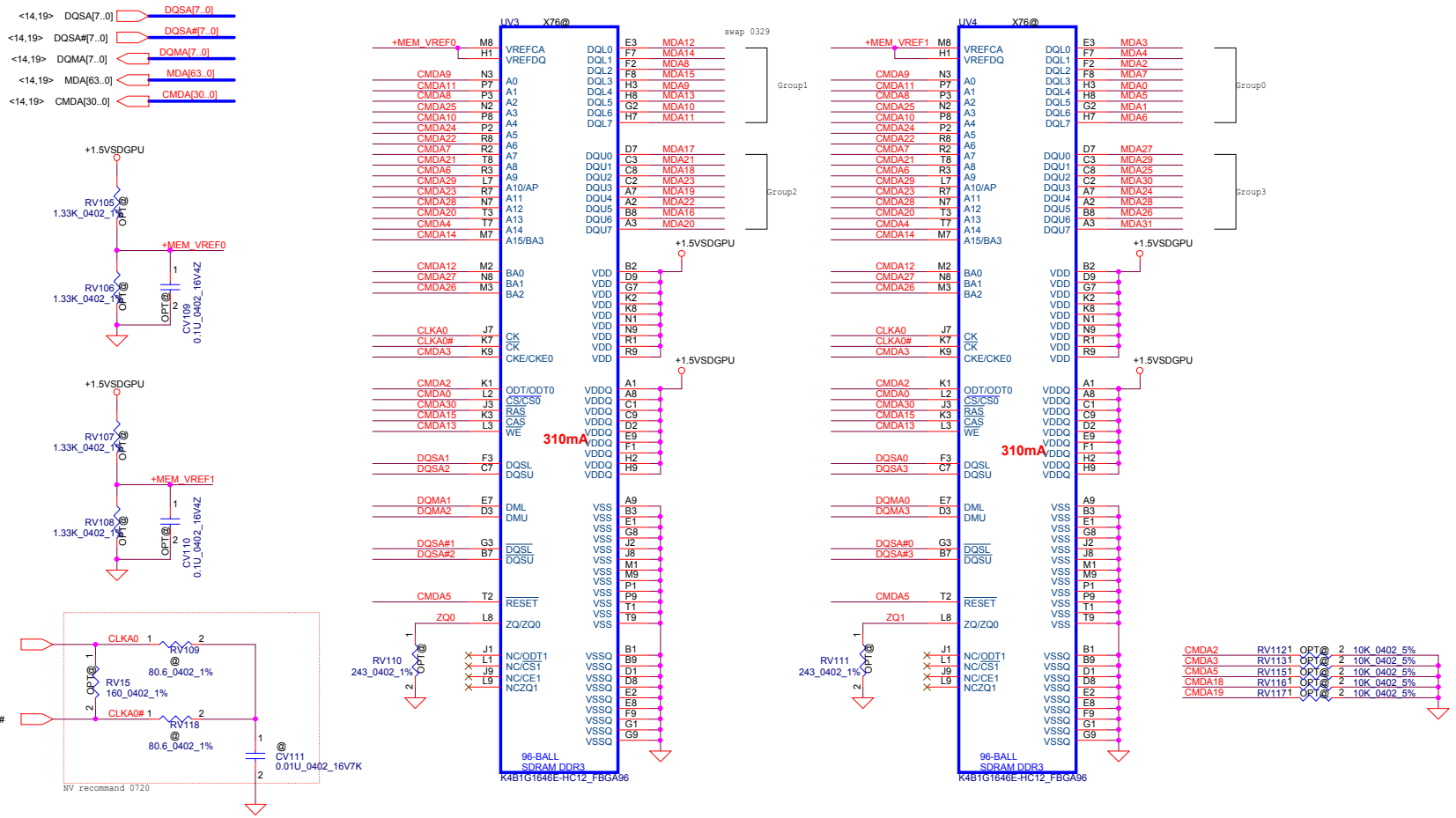
Title: N13P POWER & GND 5/9

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

Date: Wednesday, November 23, 2011 | Sheet 17 of 59

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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Title: N13P DDR3 6/9

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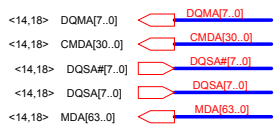
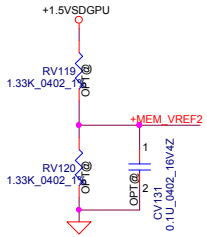
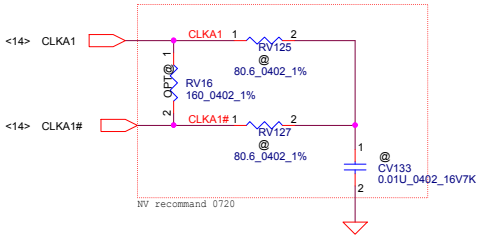
VRAM DDR3 chips (1GB)

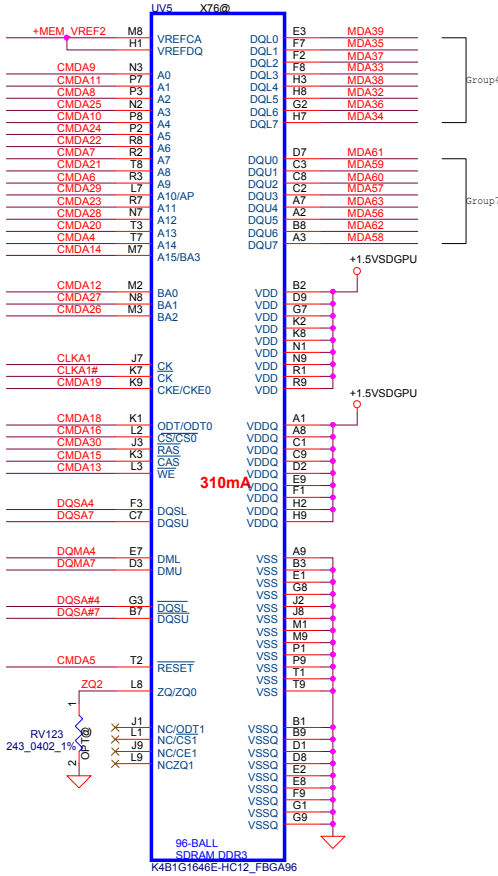
64Mx16 DDR3 *8==>1GB

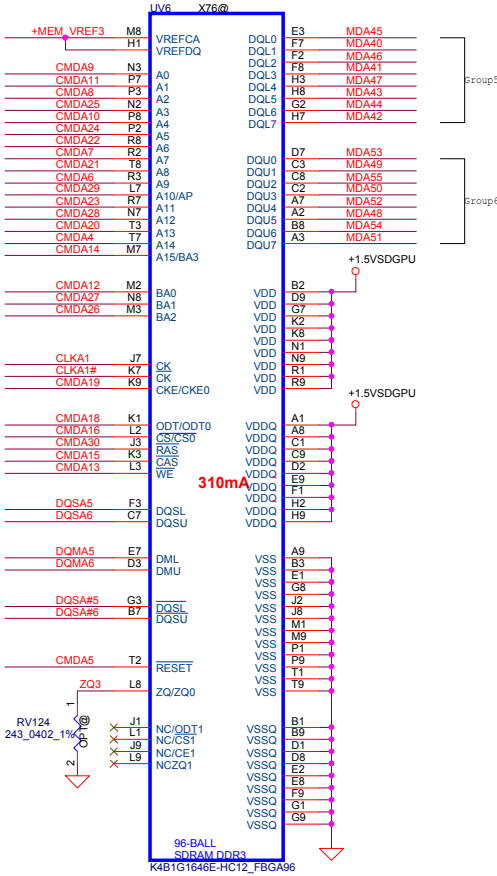
128Mx16 DDR3 *8==>2GB



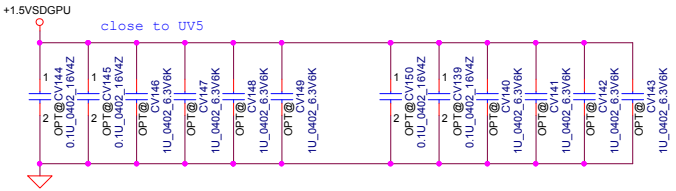


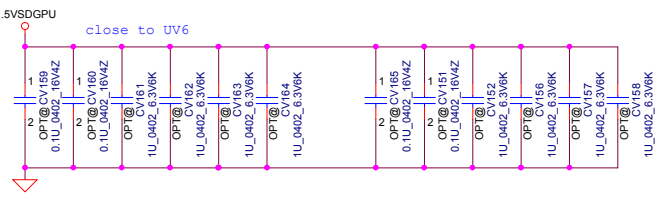






Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH





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Compal Electronics, Inc.

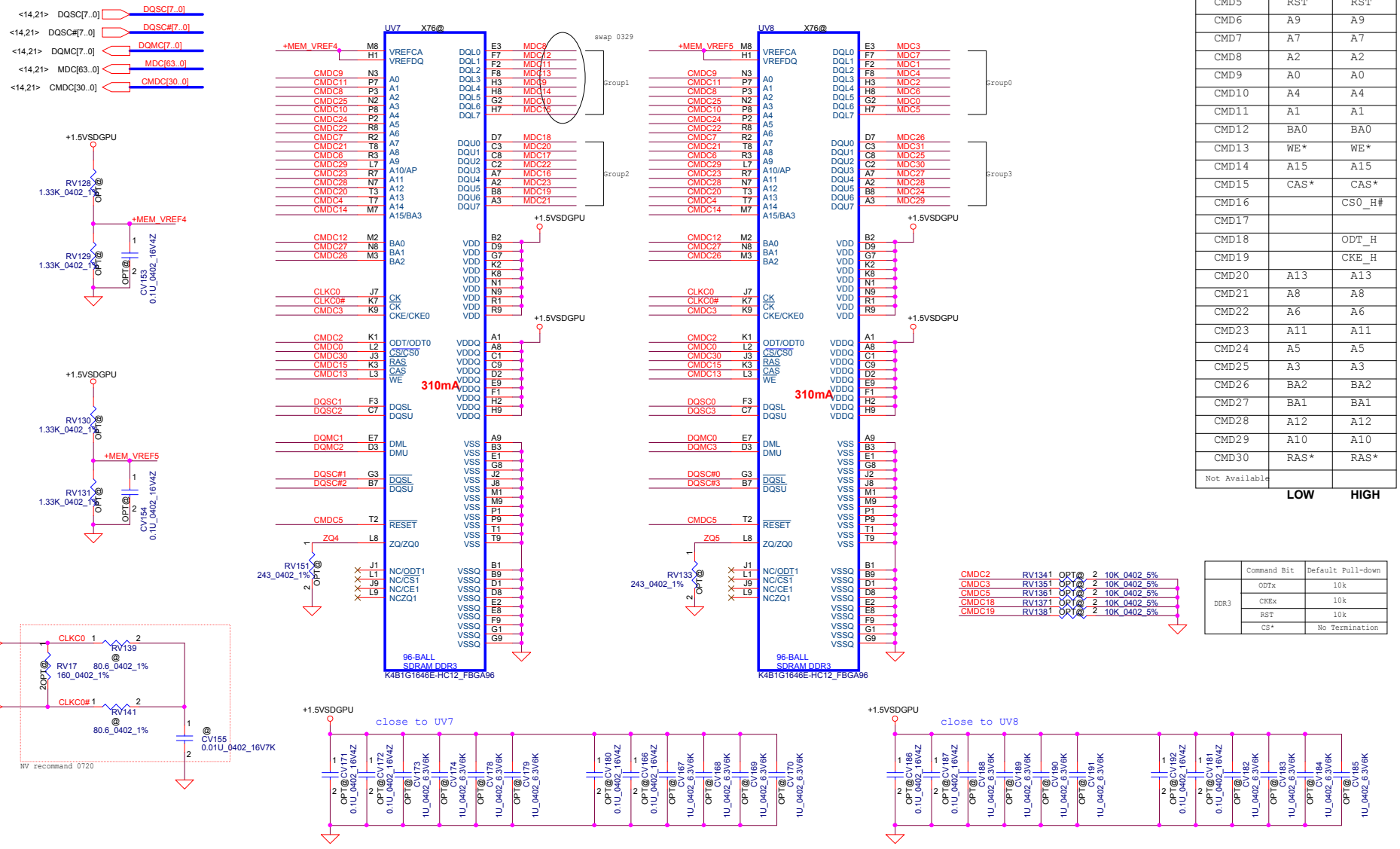
Title: N13P DDR3 7/9

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

Date: Wednesday, November 23, 2011 | Sheet 19 of 59

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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Compal Electronics, Inc.

Title: N13P DDR3 8/9

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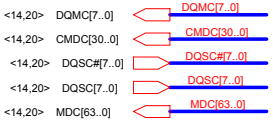
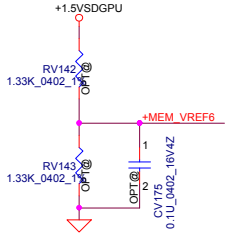
Date: Wednesday, November 23, 2011 | Sheet 20 of 59

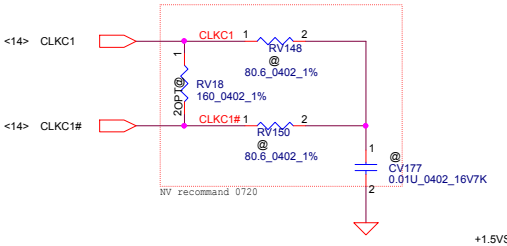
VRAM DDR3 chips (1GB)

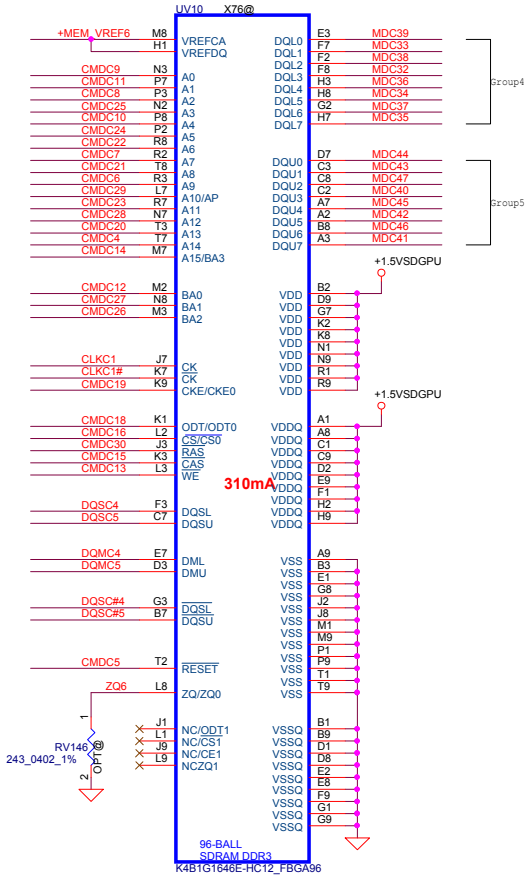
64Mx16 DDR3 *8==>1GB

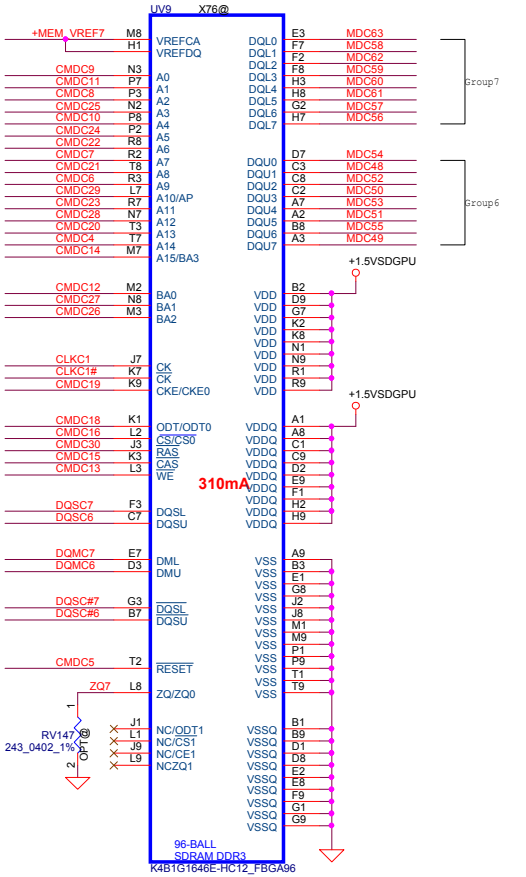
128Mx16 DDR3 *8==>2GB



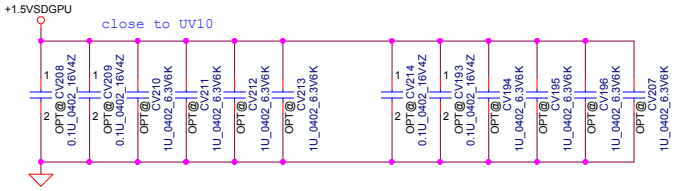


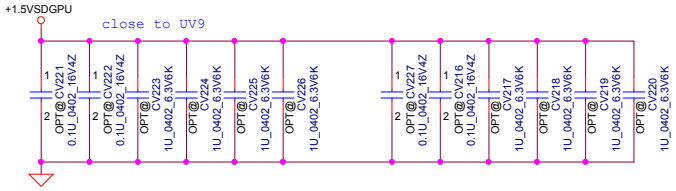






Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH





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Title: N13P DDR3 9/9

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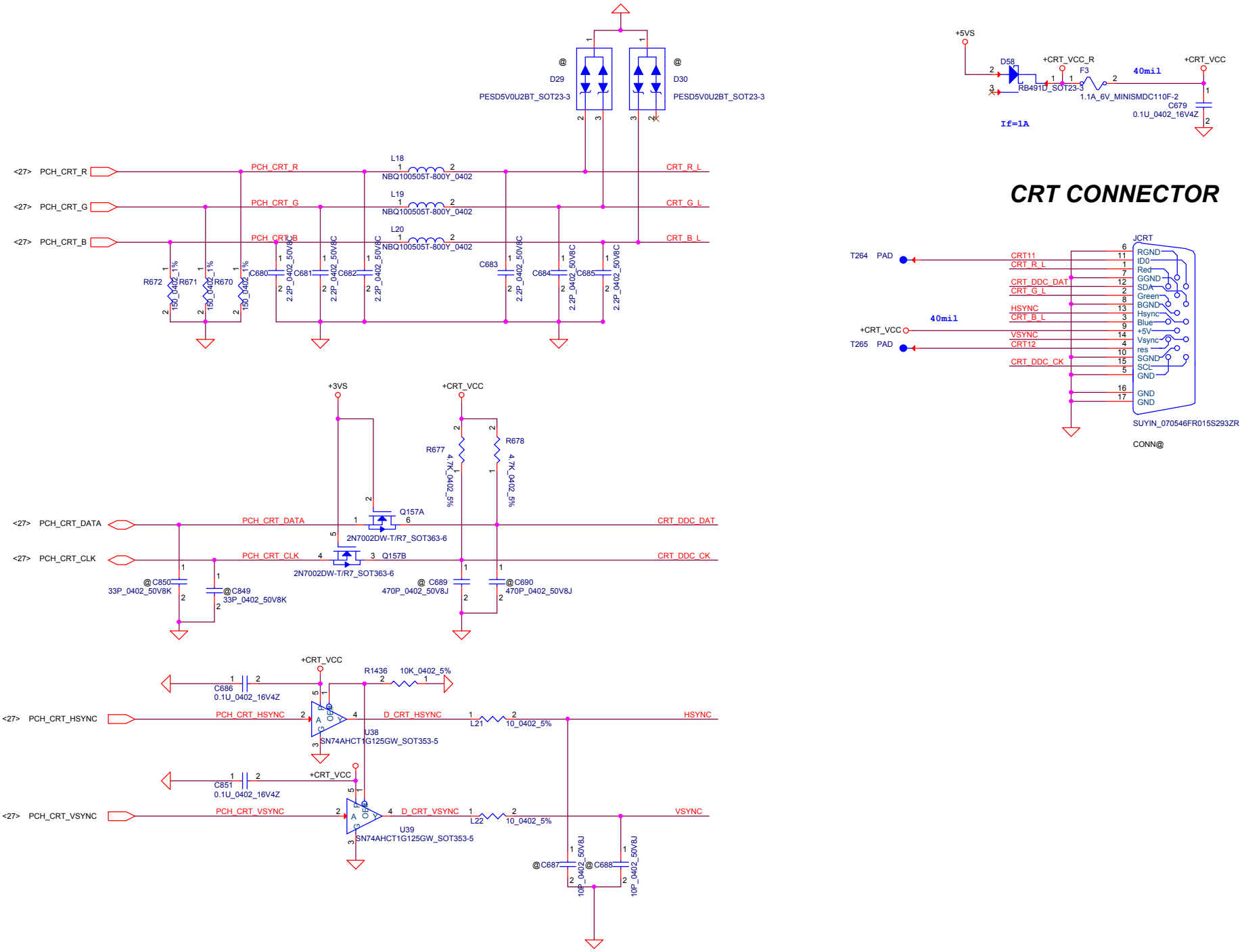

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Compal Electronics, Inc.

Title: CRT

Size | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

Date: Wednesday, November 23, 2011 | Sheet 22 of 59

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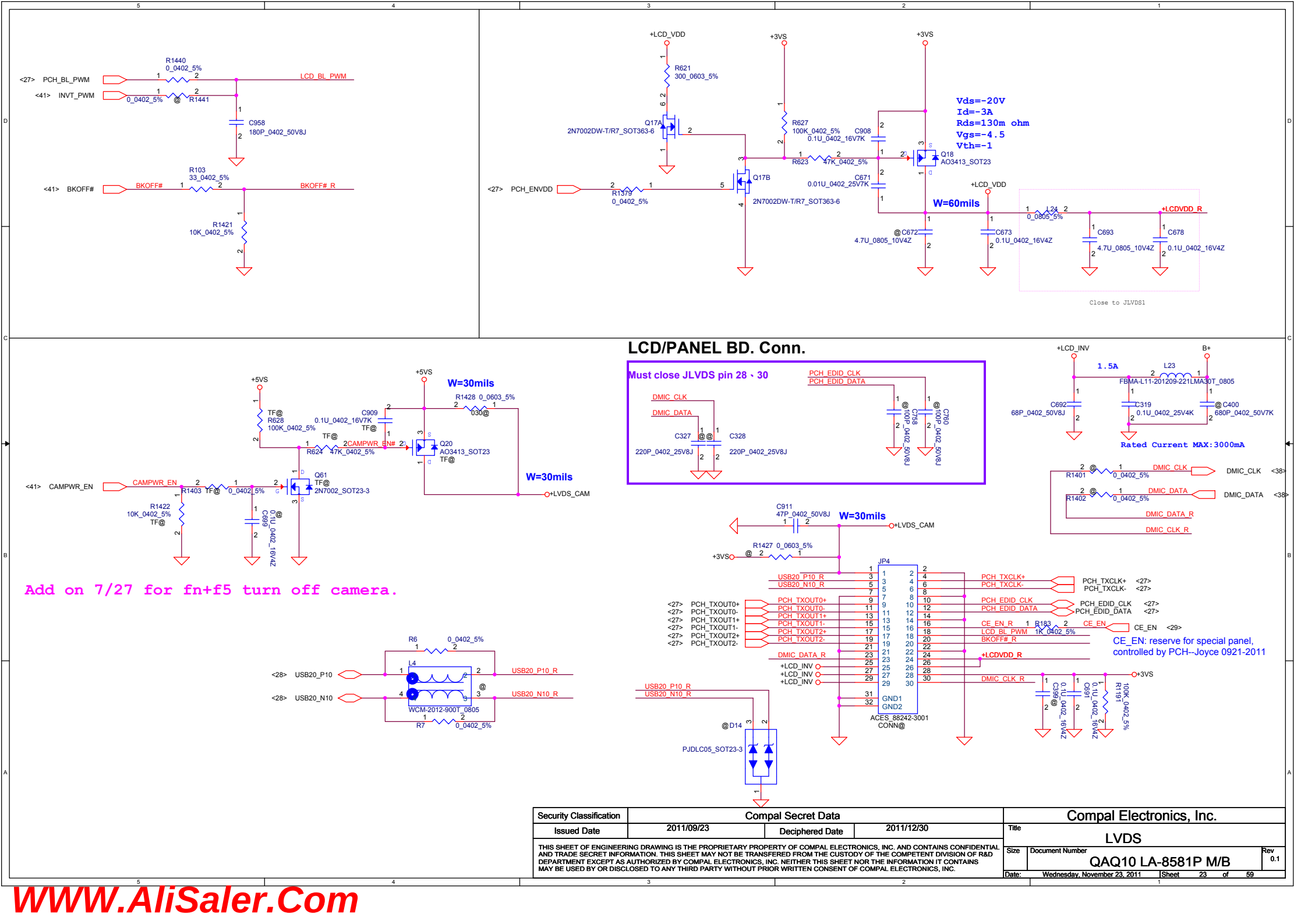

Security Classification	Compal Secret Data		
Issued Date	2011/09/23	Deciphered Date	2011/12/30

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Compal Electronics, Inc.

Title: LVDS

Size	Document Number	Rev
	QAQ10 LA-8581P M/B	0.1

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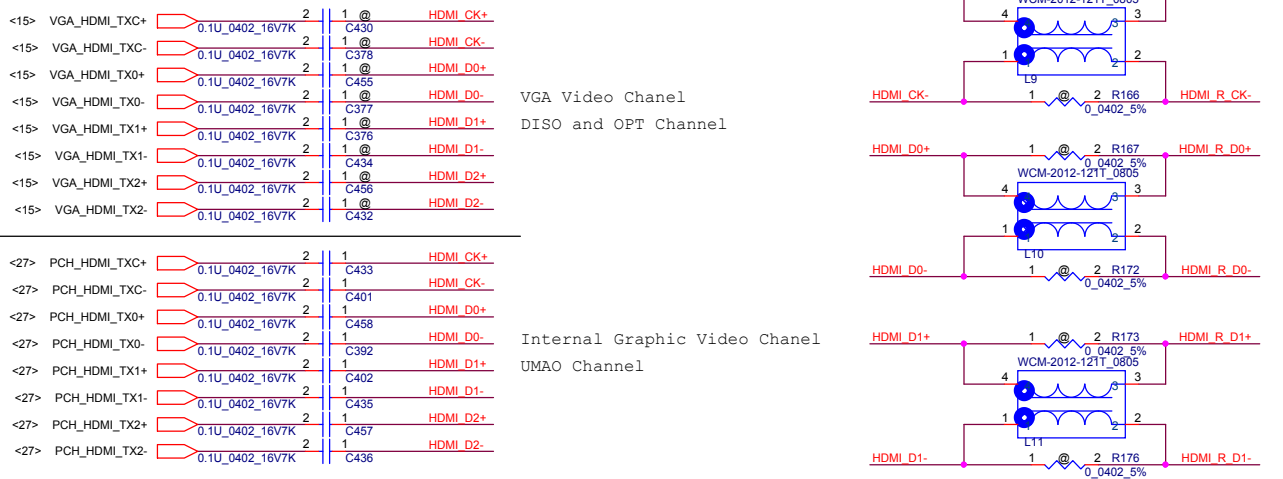
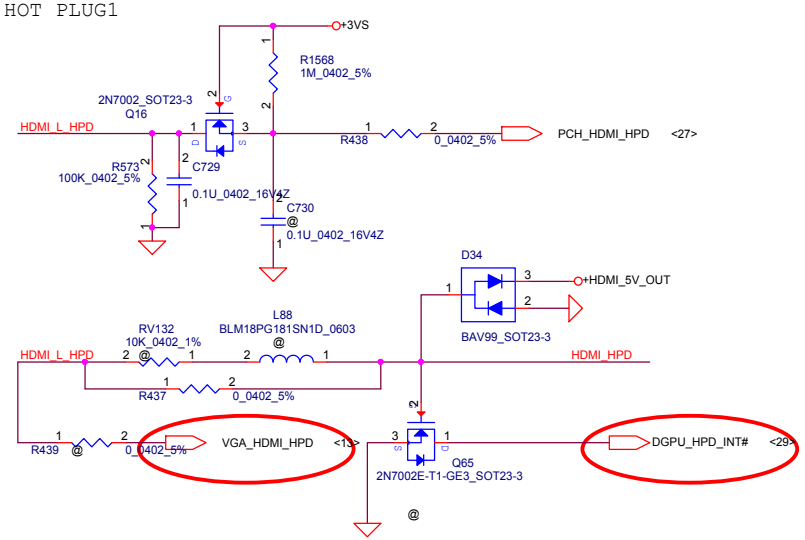
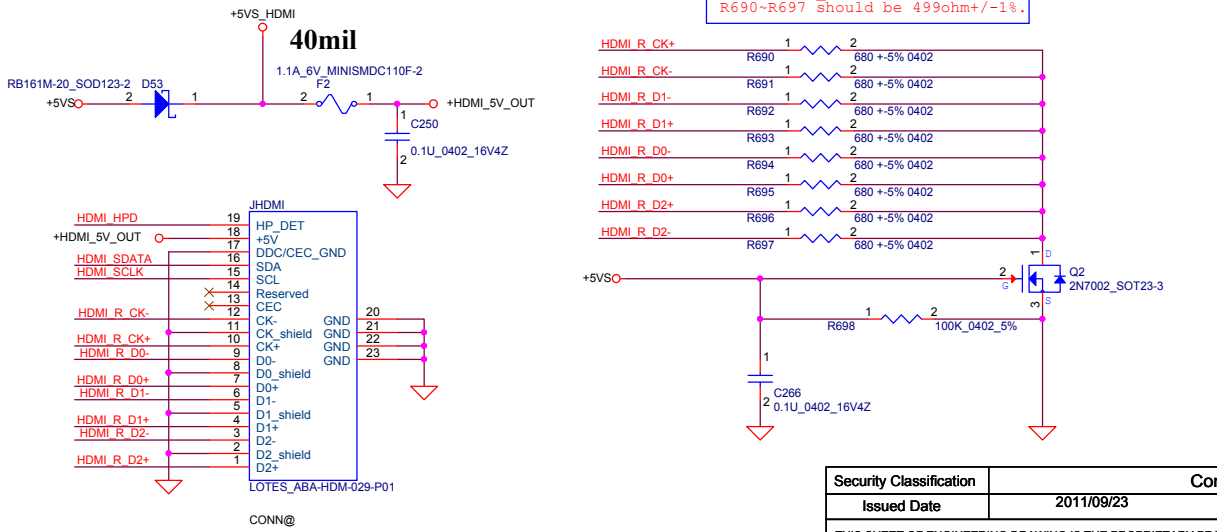
HDMI Source Select



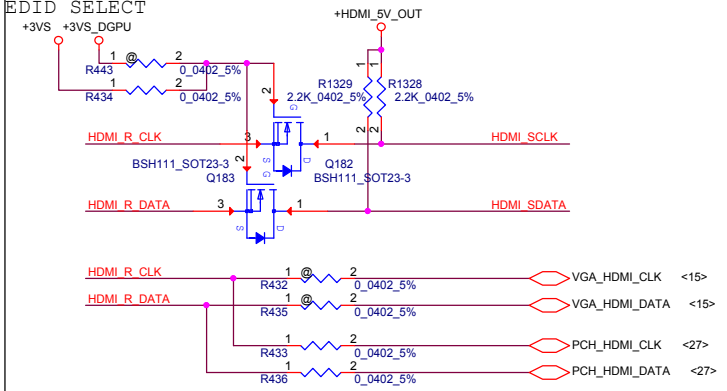
HOT PLUG1



HDMI Connector



EDID SELECT



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Compal Electronics, Inc.

Title: HDMI Connector

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Integrated SUS 1.05V VRM Enable	
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

INTVRMEN: check list Rev1.5 P63, P64 error

far away hot spot

JCMOS & JME1 place near DIMM

Place near PCH

ME_EN from EC.
Please place close to RH29 aviod the branch.

LOW=Default
★HIGH=No Reboot

HDA_SDO

ME debug mode , this signal has a weak internal PD

L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden

★Low = Disabled
High = Enabled

SATA1GP/GPIO19: Integrated 20K pull up.

SATA0GP / GPIO21: Serial ATA 0 General Purpose.
This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0.
When used as an interlock switch status indication, this signal should be drive to &0* to indicate that
the switch is closed and to &1* to indicate that the switch is open.
If interlock switches are not required, this pin can be configured as GPIO21.

SATA1GP/GPIO19: Boot BIOS Strap bit 0 (BBS0)
GNT1#/GPIO51: Boot BIOS Strap bit 1 (BBS1)

GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
Bit 11 (BBS1)	Bit 10 (BBS0)	Boot BIOS Destination
0	1	Reserved
1	0	PCI
1	1	SPI ★
0	0	LPC

PCH EDS Rev1.5 P99, P98

Intel recommend

HDA_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Chief River platfrom

Intel DPDG Rev1.2 requirement.

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Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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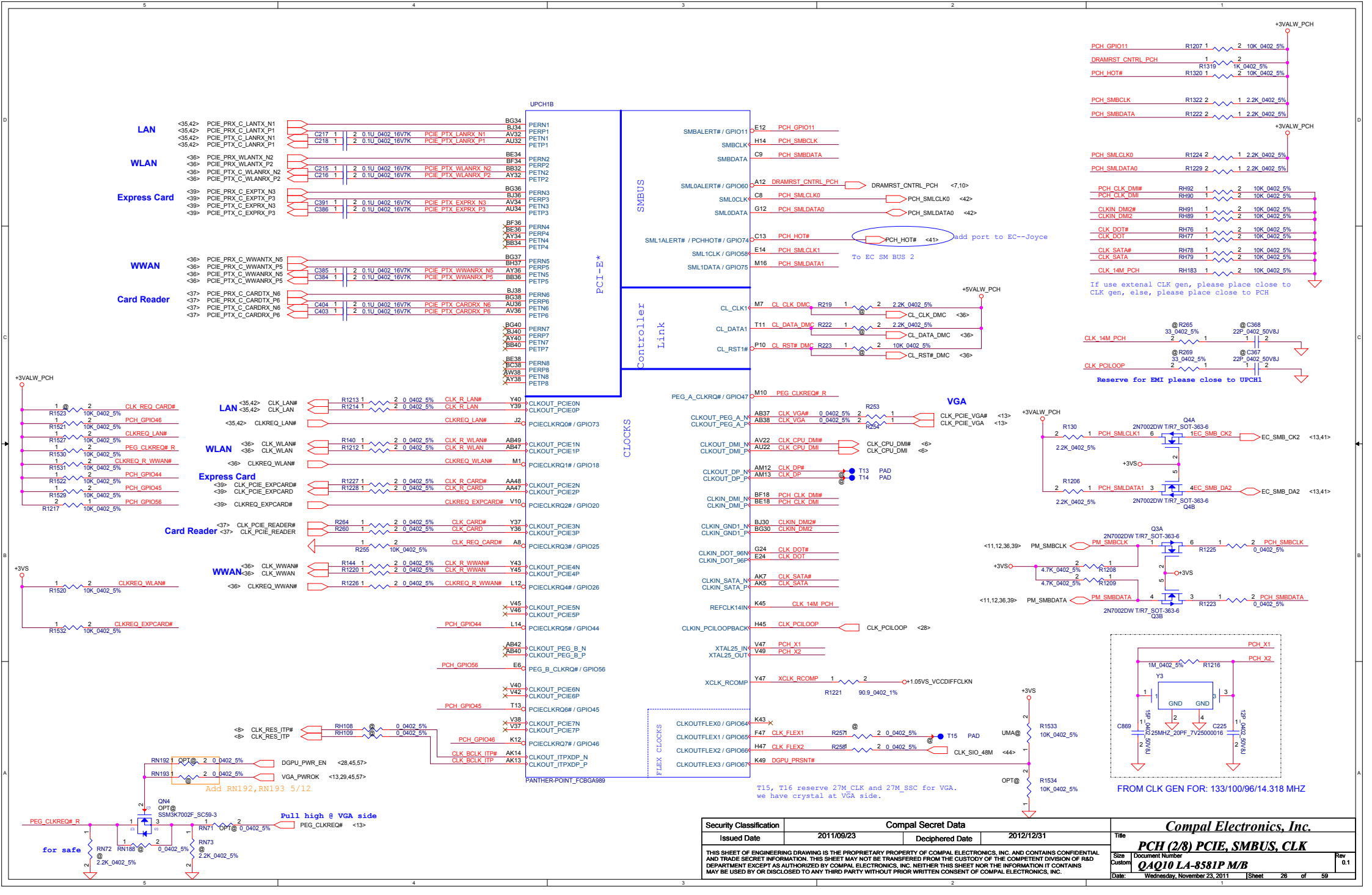

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Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	QAQ10 LA-8581P M/B	0.1

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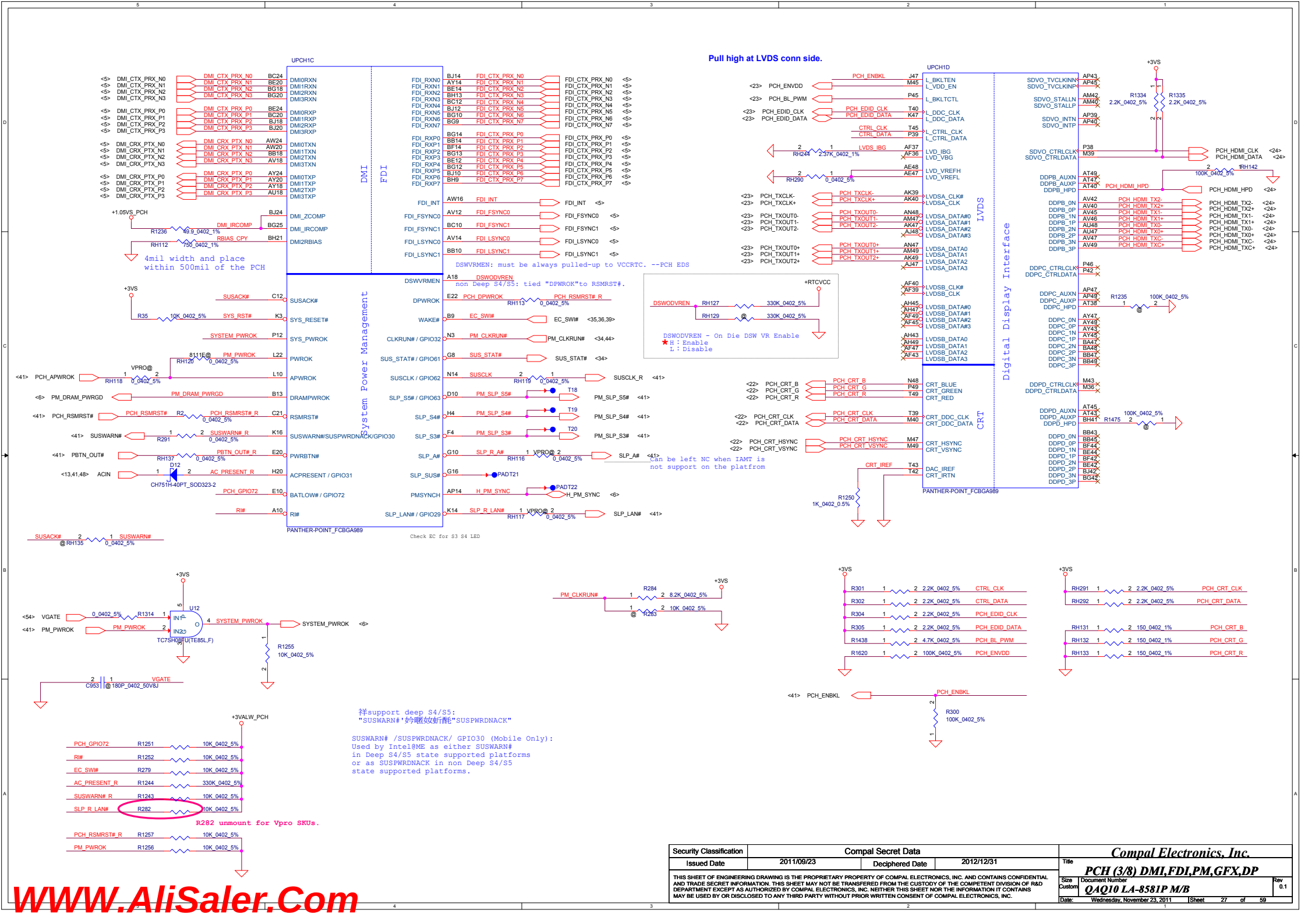

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Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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SATA1GP/GPIO19: Boot BIOS Strap bit 0 (BBS0)
GNT1#/GPIO51: Boot BIOS Strap bit 1 (BBS1)

GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
Bit 11 (BBS1)	Bit 10 (BBS0)	Boot BIOS Destination
0	1	Reserved
1	0	PCI
1	1	SPI ★
0	0	LPC

PCH EDS Rev1.5 P99, P98

Intel Anti-Theft Techonlogy

NV_ALE	
	High=Endabled
	Low=Disable(floating) ★

+1.8VS
NV_ALE @RH164 1K_0402_5%

UPCH1E

RSVD: TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24

USB3.0 Port0

USB3RN1 USB3RN2 USB3RN3 USB3RN4 USB3RP1 USB3RP2 USB3RP3 USB3RP4 USB3TN1 USB3TN2 USB3TN3 USB3TN4 USB3TP1 USB3TP2 USB3TP3 USB3TP4

<40> USB3_RX0_N
<40> USB3_RX0_P
<40> USB3_TX0_N
<40> USB3_TX0_P

PCI: PIRQA# PIRQB# PIRQC# PIRQD# REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54 GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55 PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5 PME#

CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

PLTRST#

USB: USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P

USB20_N0 <40> USB30
USB20_P0 <40>
USB20_N1 <43> L-CONN
USB20_P1 <43>
USB20_N2 <39> Smart Card
USB20_P2 <39>
USB20_N3 <44> R-CONN
USB20_P3 <44>
USB20_N4 <44> R-CONN
USB20_P4 <44>

USB port 6,7 are disabled on HM76 and HM75.

USB20_N8 <39> New Card
USB20_P8 <39>
USB20_N9 <43> USB port with Esata
USB20_P9 <43>
USB20_N10 <23> Int. Camera
USB20_P10 <23>
USB20_N11 <40> Finger Printer
USB20_P11 <40>
USB20_N12 <36> WWAN
USB20_P12 <36>
USB20_N13 <36> BT
USB20_P13 <36>

Within 500 mils
USBRBIAS# C33 USBRBIAS
RH165 22.6_0402_1%
USBRBIAS B33

OC0# / GPIO59 A14 USB_OC0# → USB_OC0# <40>
OC1# / GPIO40 K20 USB_OC1# → USB_OC1# <44>
OC2# / GPIO41 B17 USB_OC2#
OC3# / GPIO42 C16 USB_OC3#
OC4# / GPIO43 L16 USB_OC4# → USB_OC4# <40,43>
OC5# / GPIO9 A16 PCH_GPIO9
OC6# / GPIO10 D14 PCH_GPIO10
OC7# / GPIO14 C14 CP_PE# → CP_PE# <39>

For USB3.0, Left USB.
For Right power USB port
For USB port with eSATA.

PANTHER-POINT_FCBGA989

RP1: PCH_GPIO55 PCH_GPIO51 PCH_GPIO52 PCI_PIRQA# — 8.2K_0804_8P4R_5%
RP3: PCH_GPIO2 PCH_GPIO4 PCH_GPIO53 PCI_PIRQC# — 8.2K_0804_8P4R_5%
R319 DGPU_HOLD_RST#_R
R316 PCI_PIRQB#
R317 ODD_DA#
R318 DGPU_PWR_EN_R
R310 PCH_GPIO5
R311 PCI_PIRQD#
8.2K_0402_5%

DEL RP5, ADD R316,R317,R318 FOR REMOVE GPIO53 PU---0609
R1277 10K_0402_5% DGPU_PWR_EN

DGPU_HOLD_RST# R262 OPT@ 0_0402_5% DGPU_HOLD_RST#_R
<26,45,57> DGPU_PWR_EN R161 OPT@ 0_0402_5% DGPU_PWR_EN_R
<34> ODD_DA#
PLT_RST# <6,34,35,36,37,39,41,42,44> R259 0_0402_5% BUF_PLT_RST#
CLK_PCI_EC <41> R280 22_0402_5% CLK_PCI_EC_R
CLK_PCILOOP <26> R281 22_0402_5% CLK_PCI
CLK_PCI_SIO <44> R285 22_0402_5% CLK_SIO
CLK_PCI_TPM <34> R286 22_0402_5% CLK_TPM

U8 TC7SH08FU(TE85L,F)
BUF_PLT_RST# → PLT_RST#
R157 100K_0402_5%
R151 100K_0402_5%
+3VS_DGPU
C477 0.1U_0402_16V4Z OPT@
U20 TC7SH08FU(TE85L,F)
DGPU_HOLD_RST#
R261 OPT@ 0_0402_5%
PLTRST_VGA# <13>
R413 1K_0402_5% OPT@
RV49 10K_0402_5% @
R165 100K_0402_5% OPT@

+3VALW_PCH
USB_OC3# R1270 10K_0402_5%
USB_OC4# R1271 10K_0402_5%
USB_OC2# R1268 10K_0402_5%
USB_OC0# R1267 10K_0402_5%
USB_OC1# R1269 10K_0402_5%
CP_PE# R1306 10K_0402_5%
PCH_GPIO9 R1307 10K_0402_5%
PCH_GPIO10 R1308 10K_0402_5%

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Compal Electronics, Inc.
Title: PCH (4/8) PCI, USB, NVRAM
Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1
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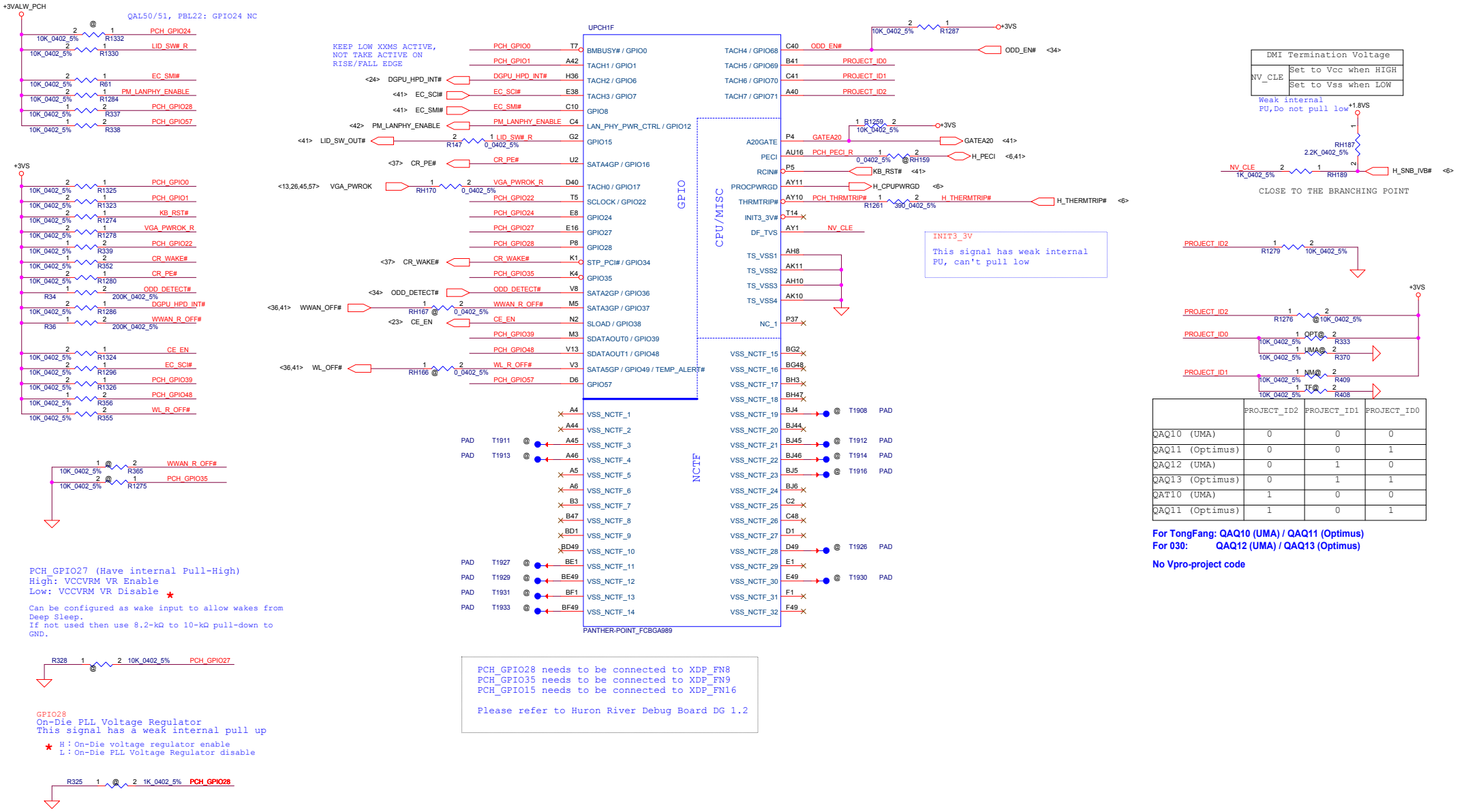

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QAQ10 (UMA)	0	0	0
QAQ11 (Optimus)	0	0	1
QAQ12 (UMA)	0	1	0
QAQ13 (Optimus)	0	1	1
QAT10 (UMA)	1	0	0
QAQ11 (Optimus)	1	0	1

For TongFang: QAQ10 (UMA) / QAQ11 (Optimus)
For 030: QAQ12 (UMA) / QAQ13 (Optimus)

No Vpro-project code

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Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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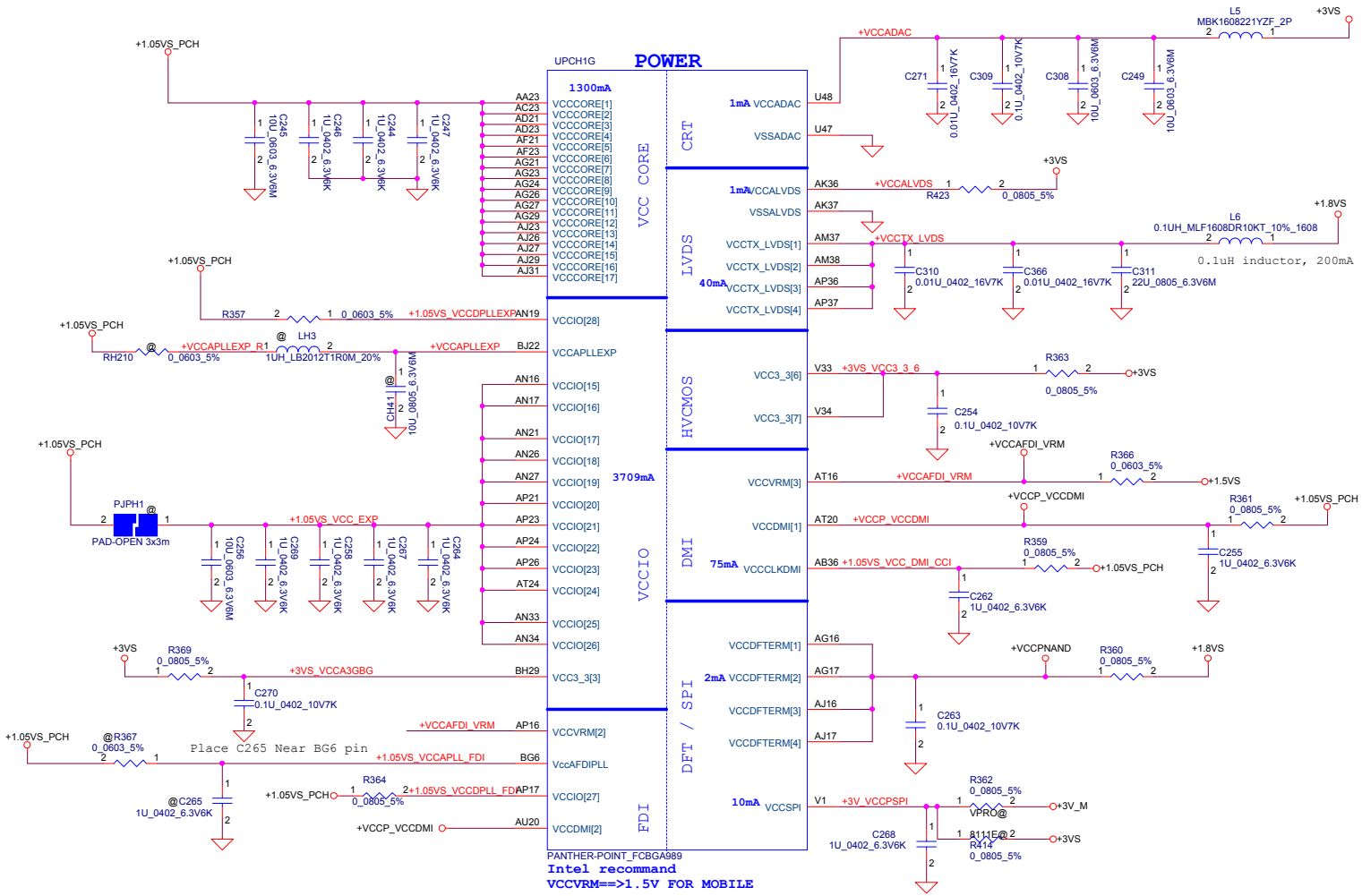

PCH Power Rail Table Refer to PCH EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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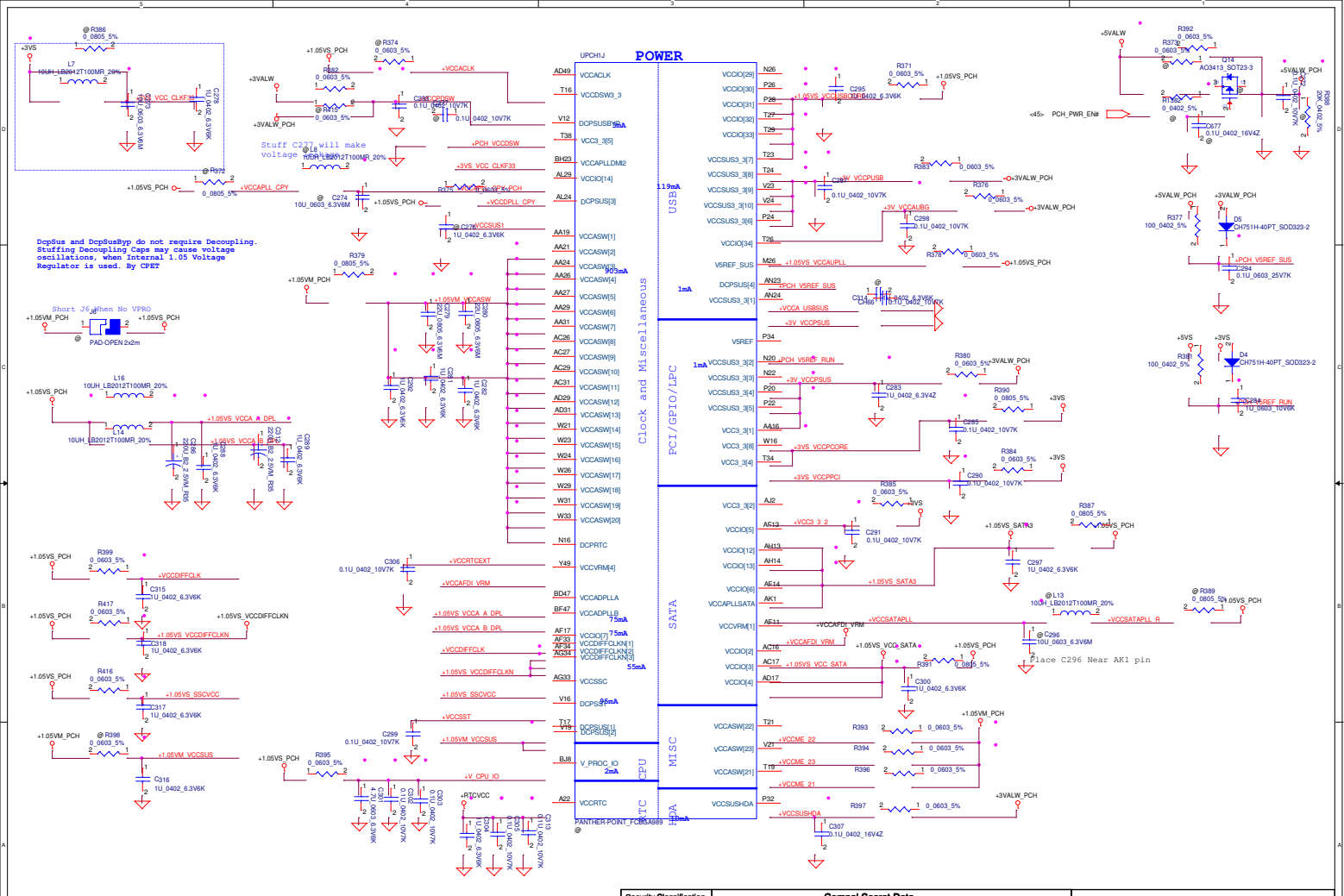

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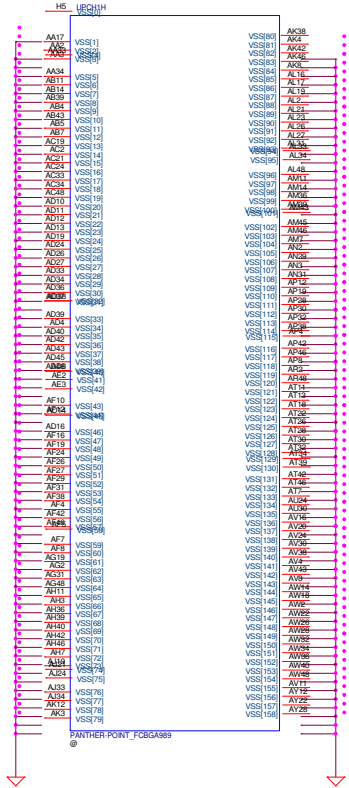

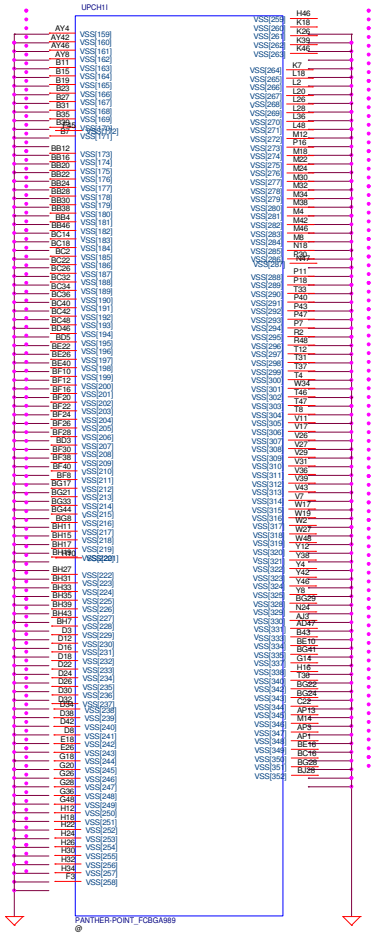

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Title		
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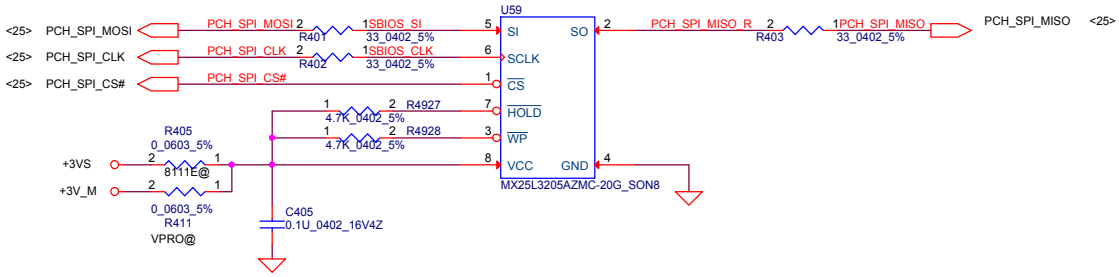
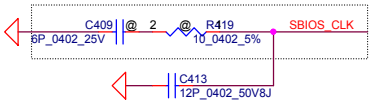
SBIOS SPI Flash



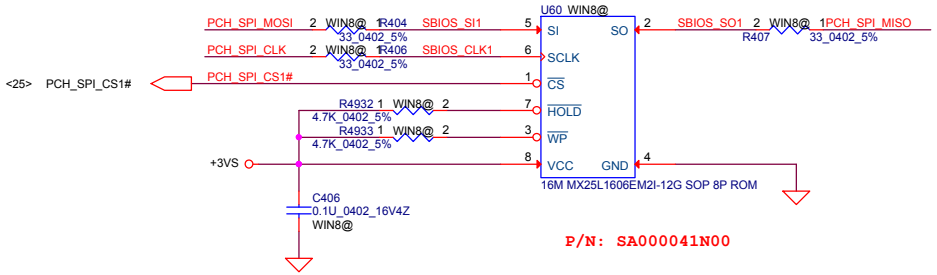
For EMI resuest.



U59:

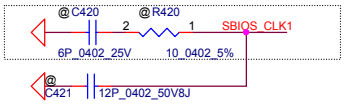
Vpro--SA000039A00	8MB
non-Vpro--SA00003K80	4MB

BIOS SPI Flash (2MByte*1) For Win8



P/N: SA000041N00

For EMI resuest.



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Compal Electronics, Inc.

Title: SBIOS/EC ROM

Size | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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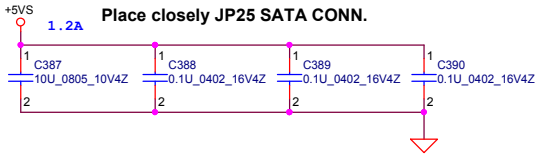
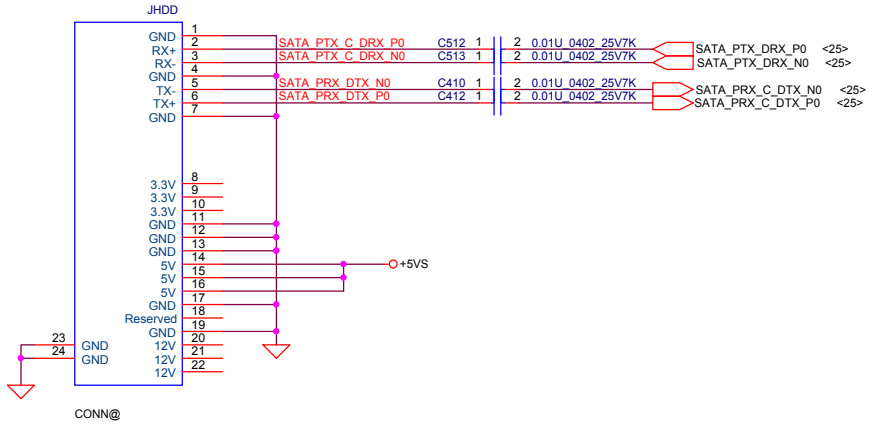
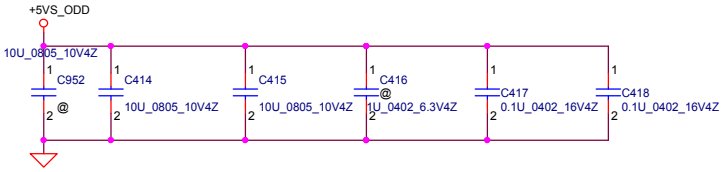
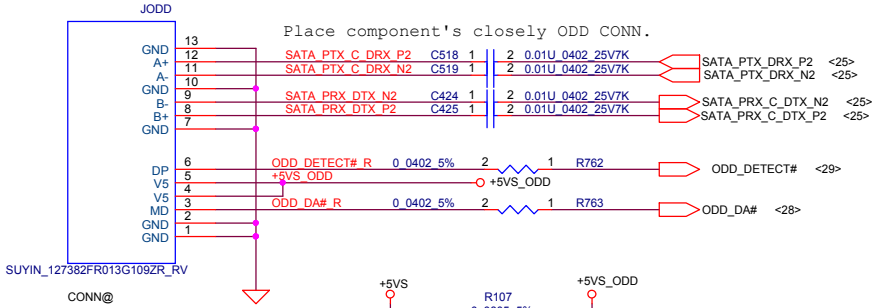
SATA HDD Conn.

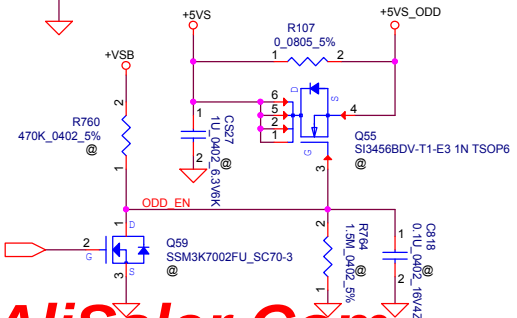




SATA ODD Conn







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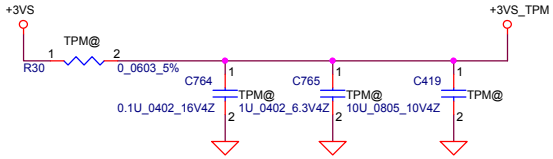
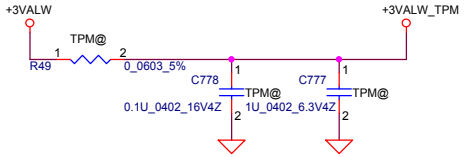
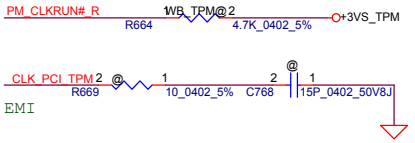
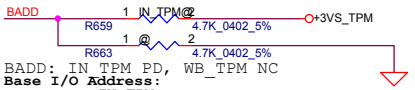
TPM 1.2









BADD: IN_TPM PD, WB_TPM NC

Base I/O Address:

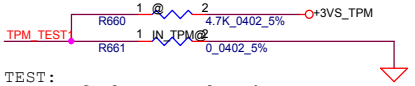
IN_TPM:

0 = 02Eh * 1 = 04Eh

WB_TPM:

Default:7EH-7FH

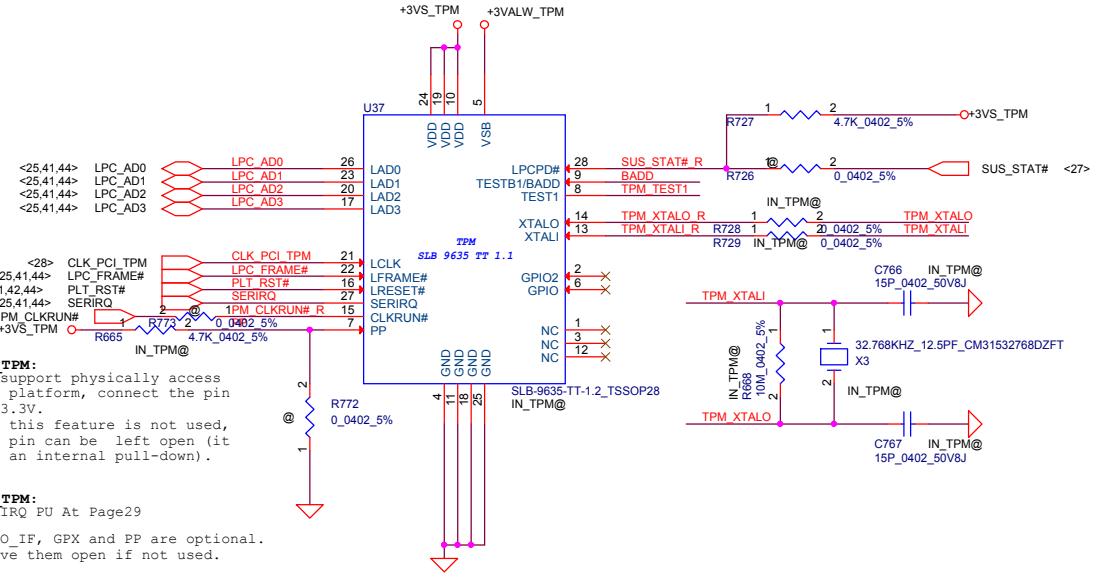
4.7K PD:EEH-EFH



TEST:

Default: Normal Mode, IN_TPM PD, WB_TPM NC

4.7K PU: Test Mode



IN_TPM:
if support physically access the platform, connect the pin to 3.3V.
If this feature is not used, the pin can be left open (it has an internal pull-down).

WB_TPM:
SERIRQ PU At Page29

GPIO_IF, GPX and PP are optional.
Leave them open if not used.

U37

S IC WPCT200AA0WG TSSOP 28P TPM
WB_TPM@

BOM
IN_TPM:IN_TPM@&TPM@
WB_TPM:WB_TPM@&TPM@

For NON_TPM SKU Reserve

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Issued Date	2011/09/23	Deciphered Date	2011/12/30

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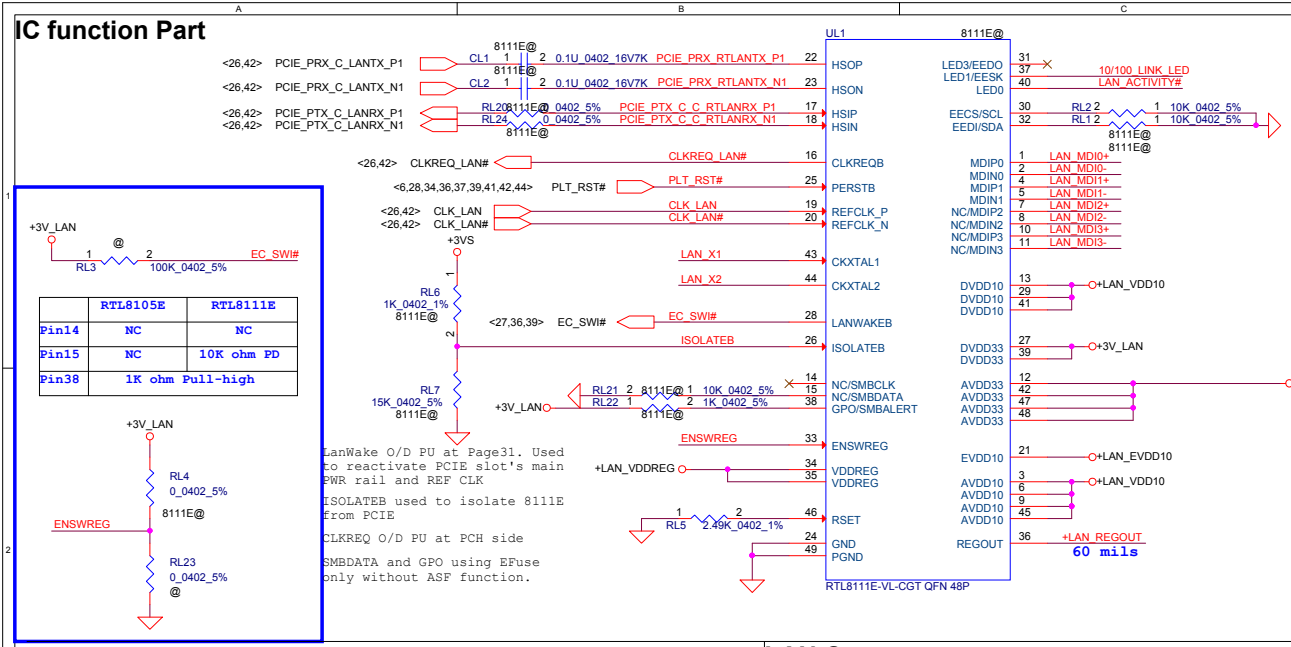
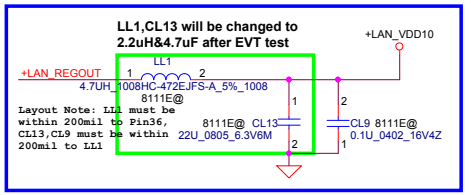
Compal Electronics, Inc.			
Title	SATA-HDD/ODD		
Size	Document Number		Rev
	QAQ10 LA-8581P M/B		0.1
Date: Wednesday, November 23, 2011	Sheet 34 of 59		

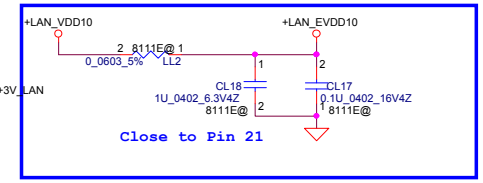
IC function Part

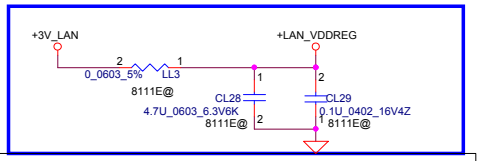


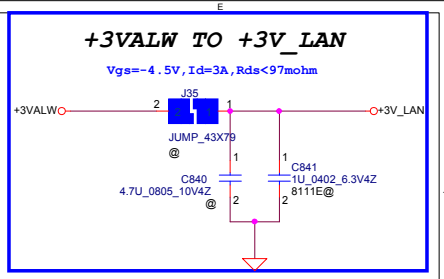
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

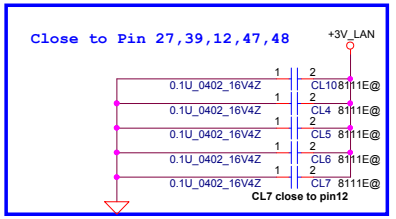
PWR

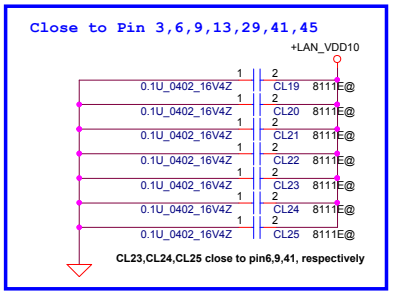




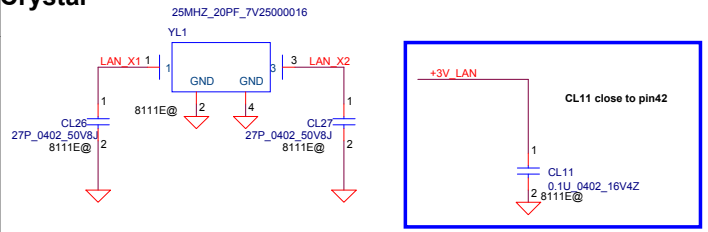




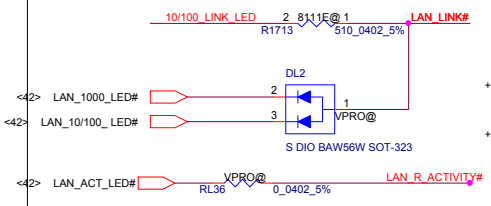


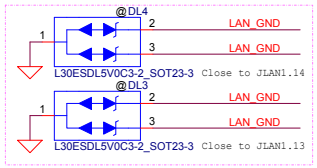


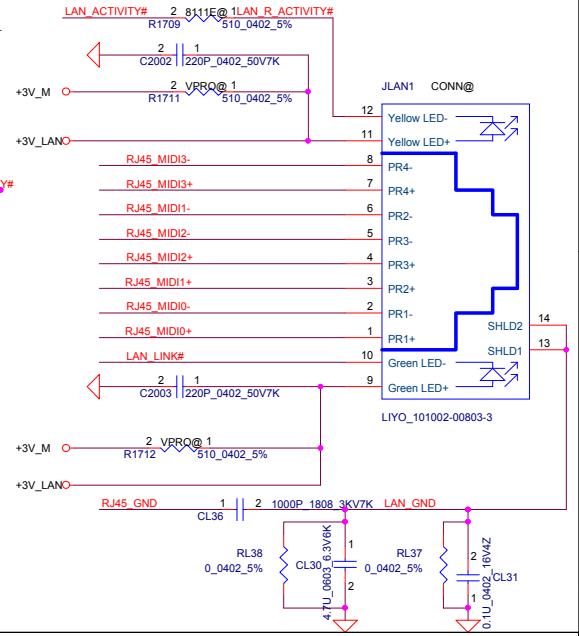
Crystal



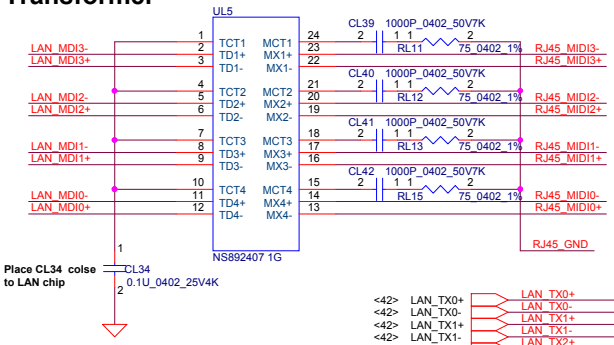
LAN Conn.

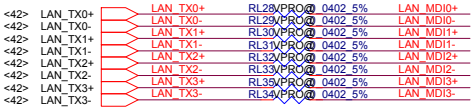






Transformer





BOM Structure

For P/N and footprint
Please place them to ISPD page

UL1
8105E 10/100M
8105E@

UL5
10/100M transformer
8105E@

8105:
RL22,CL39,RL11,CL40,RL12,CL23,CL24,CL25,CL7UNSTUFF

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PCIe-LAN-RTL8105E/8111E

Size: Custom | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

Date: Wednesday, November 23, 2011 | Sheet 35 of 59

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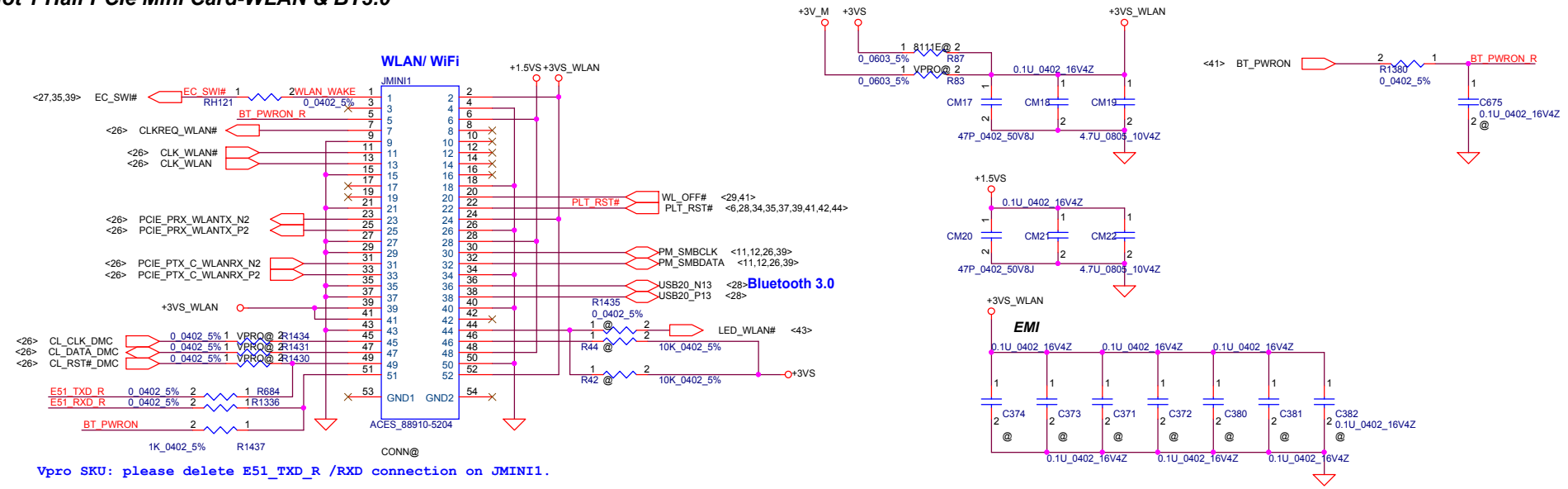
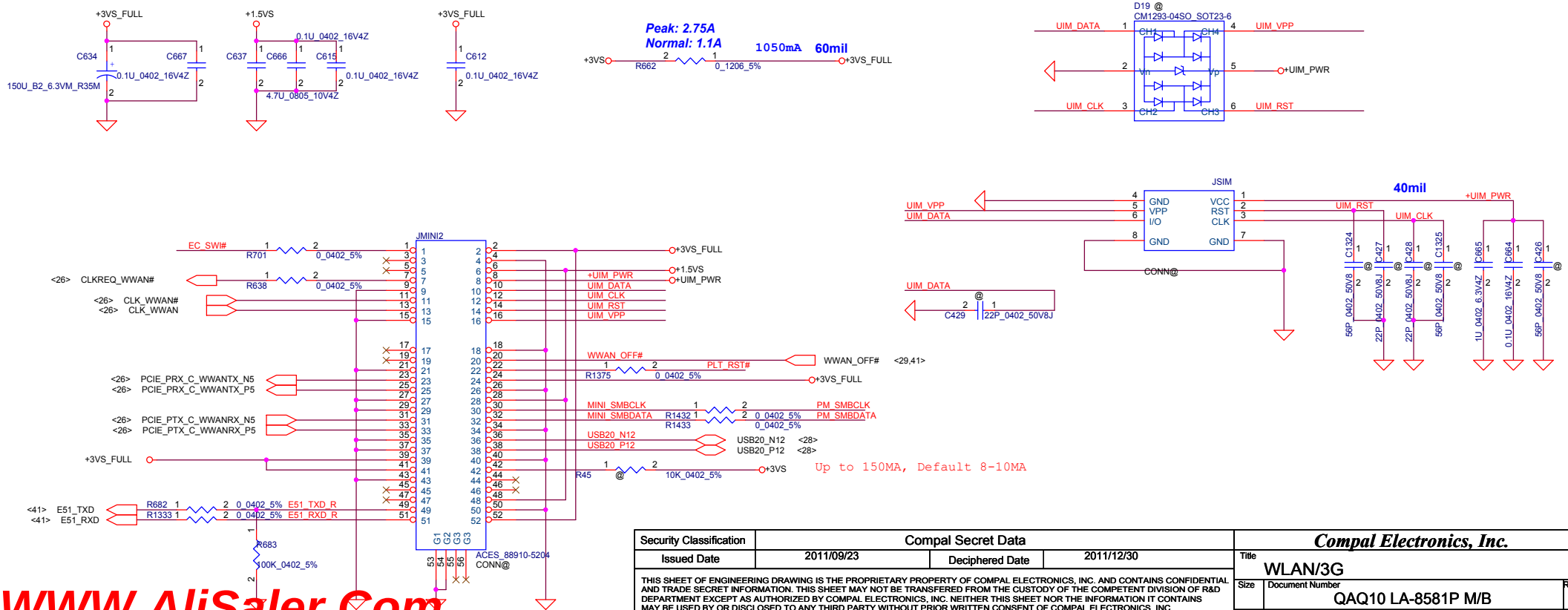
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Slot 2 Half PCIe Mini Card-G/GPS (FULL Card)



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Compal Electronics, Inc.

Title: WLAN/3G

Size: | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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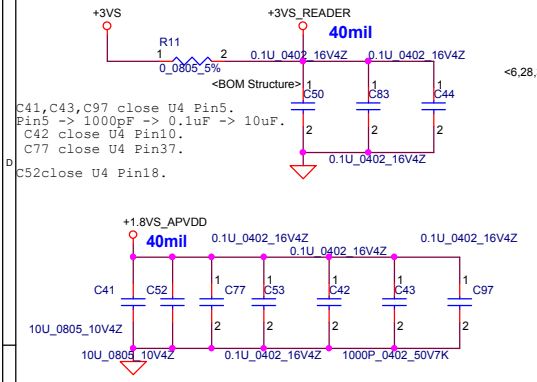
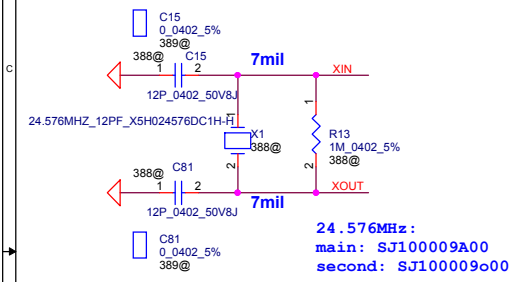
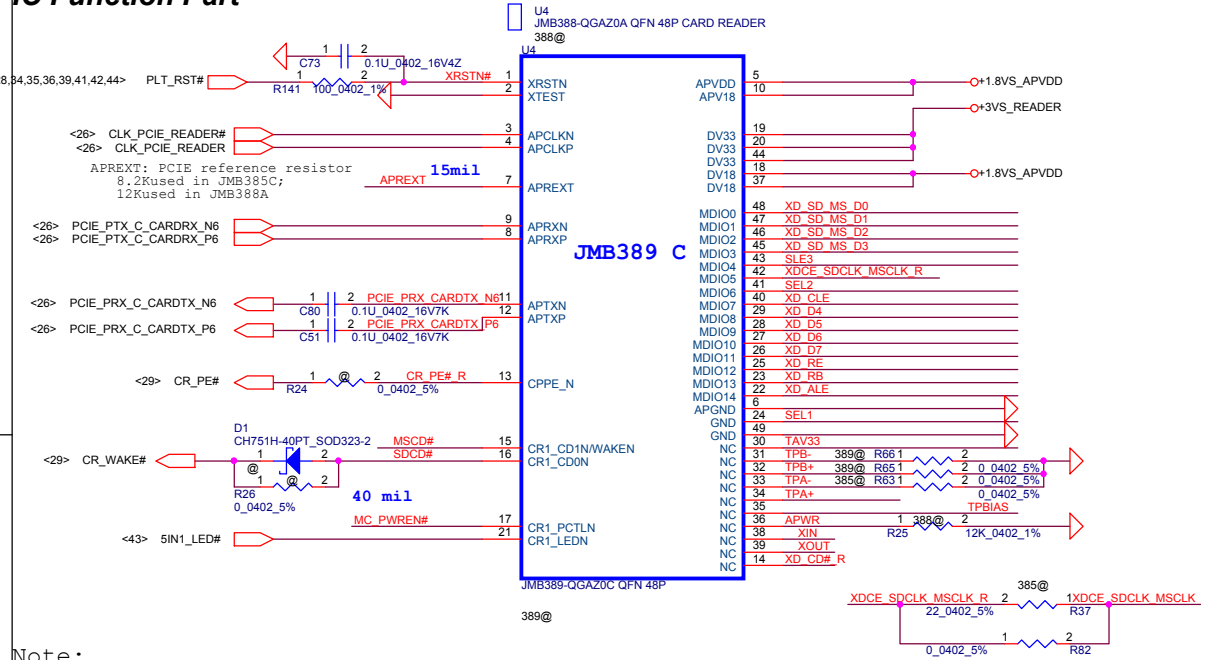
IC PWR



External Crystal

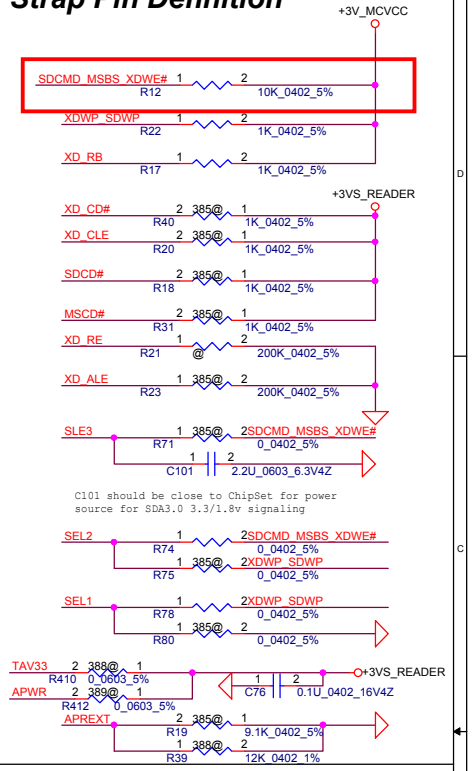


IC Function Part

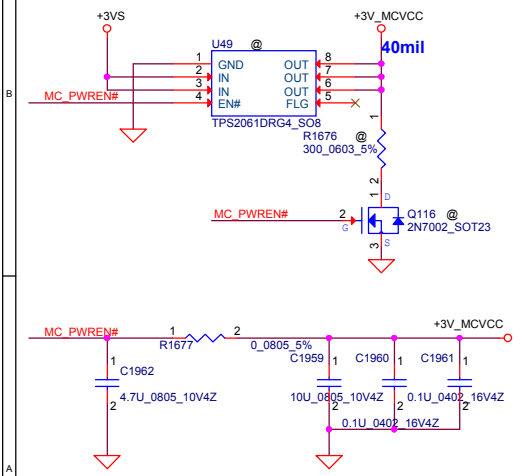


Note:
Colay With JMB385; W/1394, mount JMB388;WO/1394, mount JMB385.
CR_PE# and CR_WAKE reserve for D3 mode

Strap Pin Definition



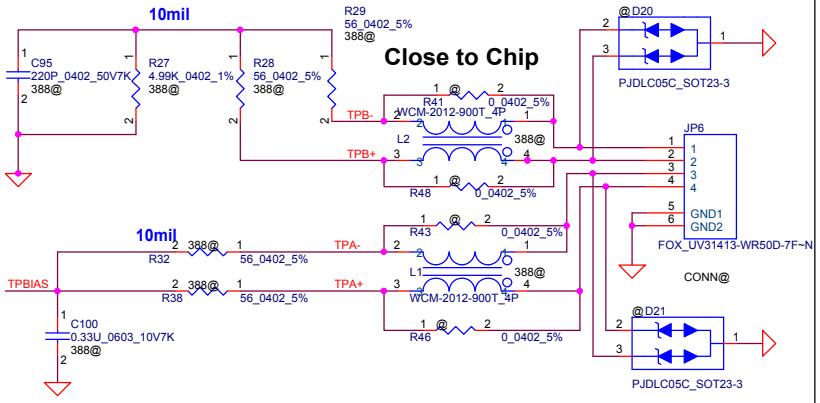
Memory Card Power



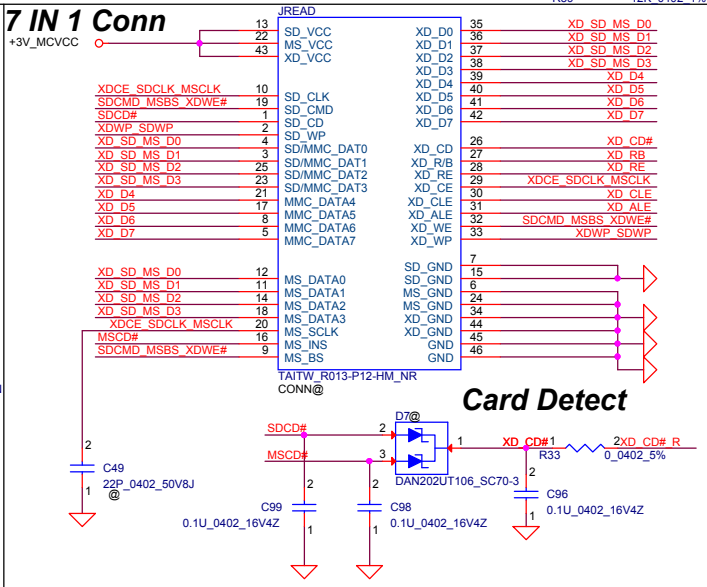
Note:

if use external PWR and change +3V_MCPWR as control signal, Need BIOS to change the Setting.

1394 Conn



7 IN 1 Conn



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Compal Electronics, Inc.

Title: Card Reader

Size | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

Date: Wednesday, November 23, 2011 | Sheet 37 of 59

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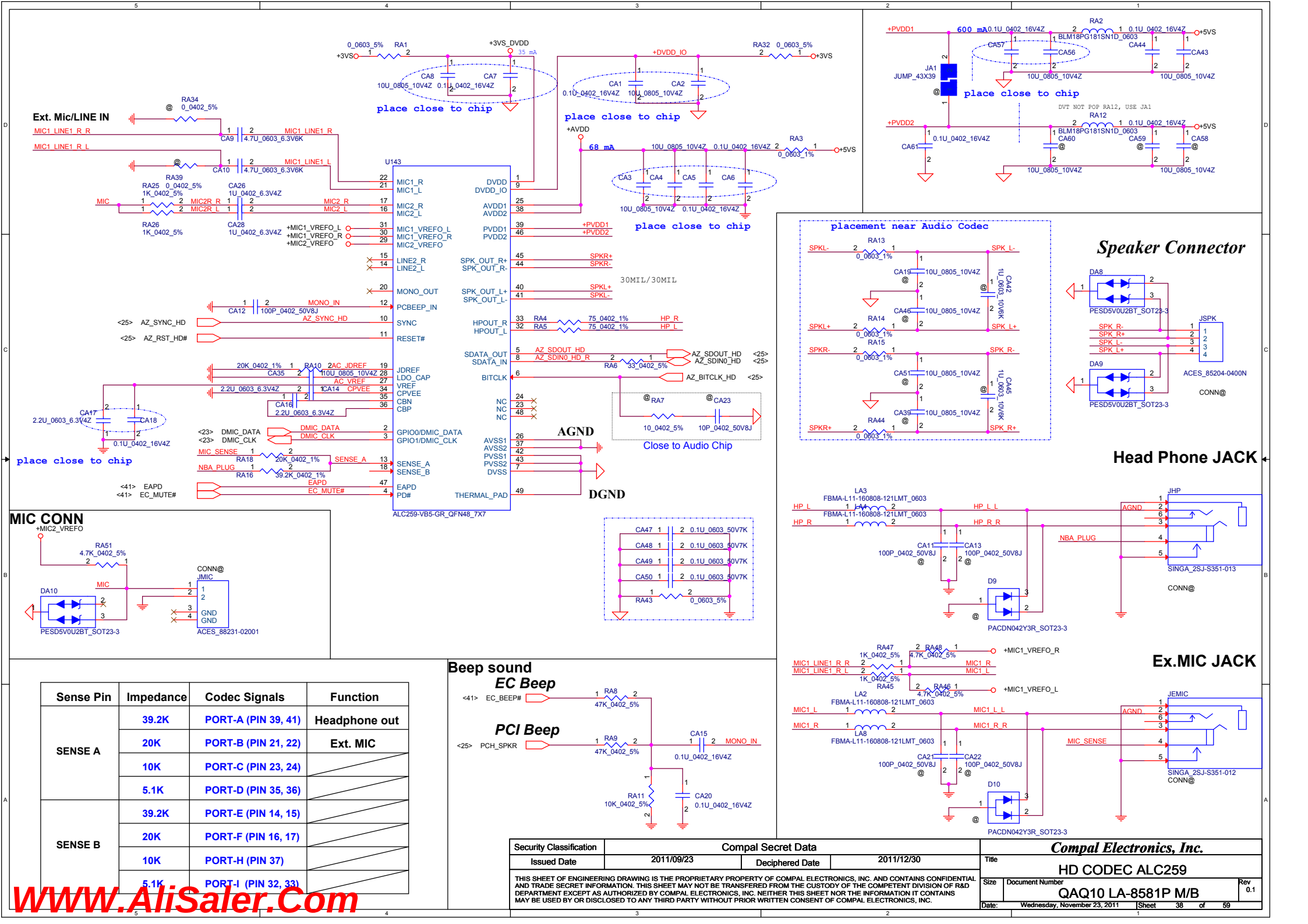

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	

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Compal Electronics, Inc.

Title: HD CODEC ALC259

Size: | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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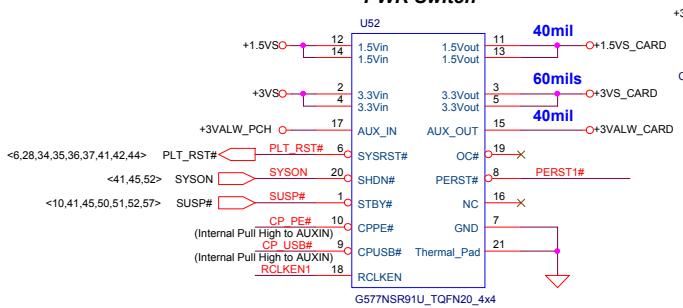
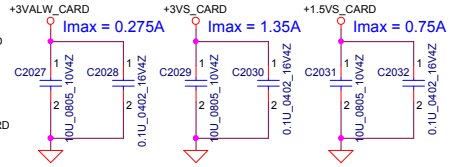
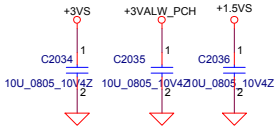
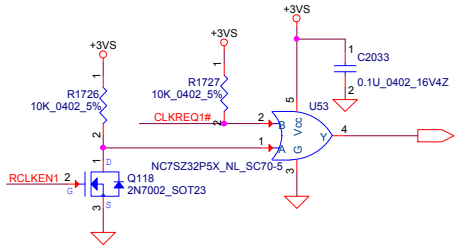
Express Card

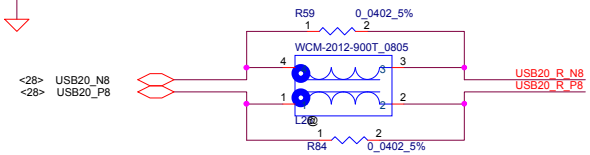
PWR Switch



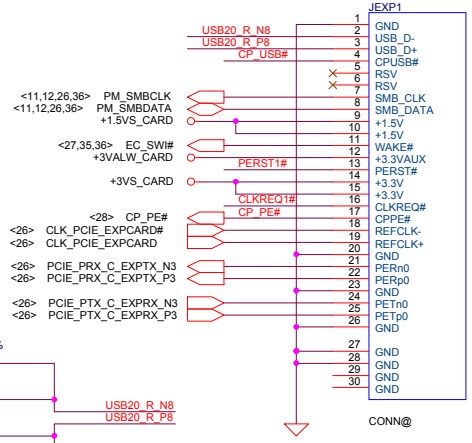






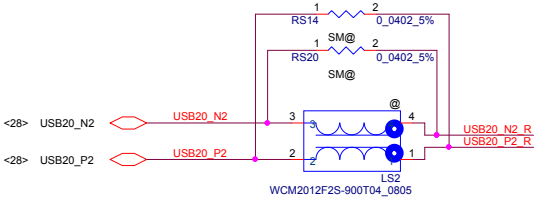


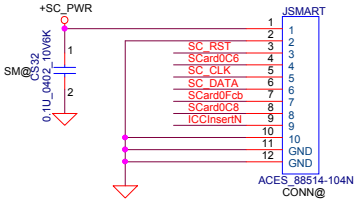
New Card Socket (Left/TOP)

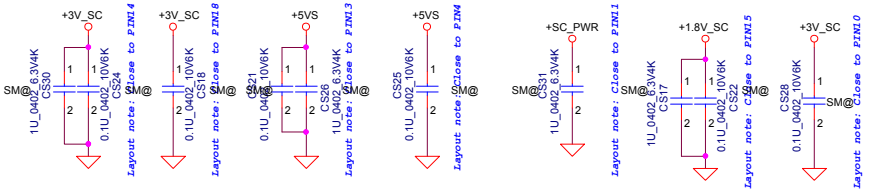


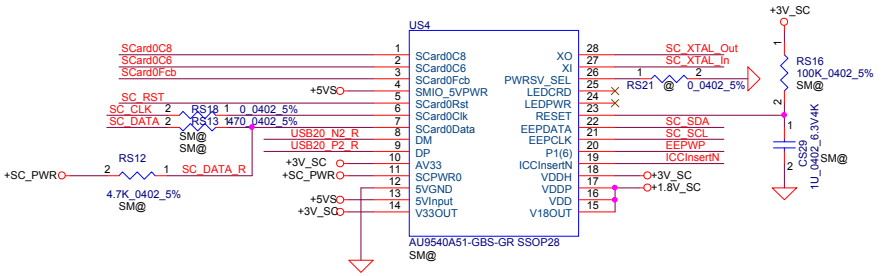
Smart Card

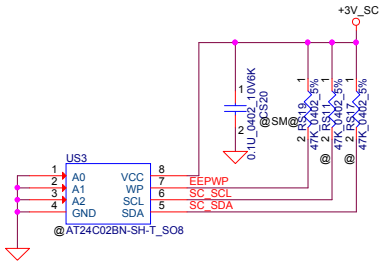
This pin1 define need check

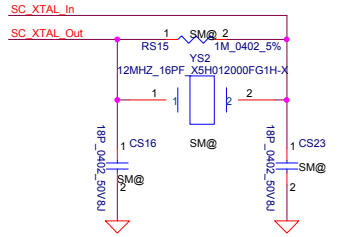












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Issued Date	2011/09/23	Deciphered Date	2011/12/30

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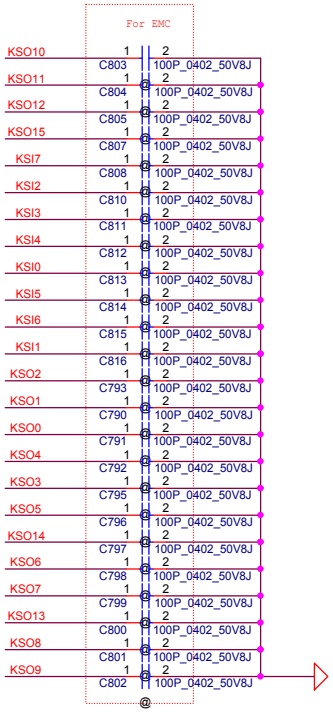
Compal Electronics, Inc.

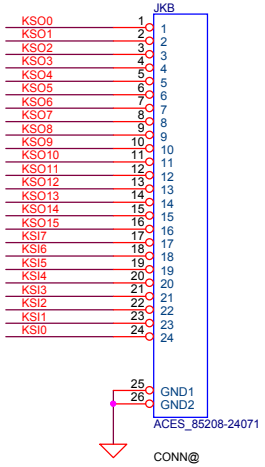
Title: Express Card

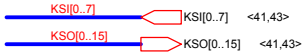
Size: B | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

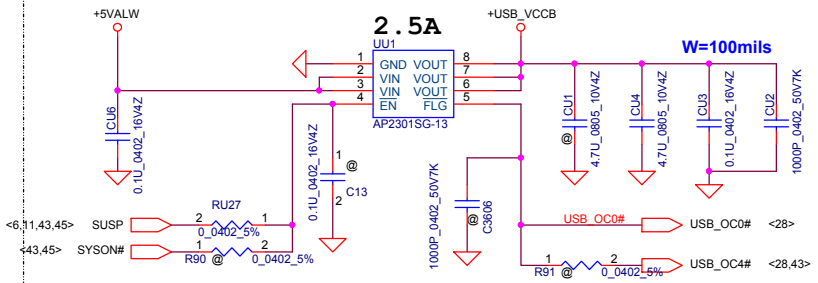
Date: Wednesday, November 23, 2011 | Sheet 39 of 59

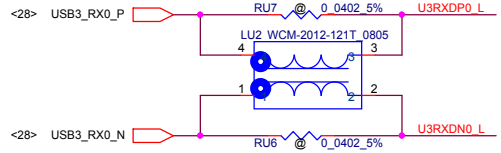
KEYBOARD CONN.

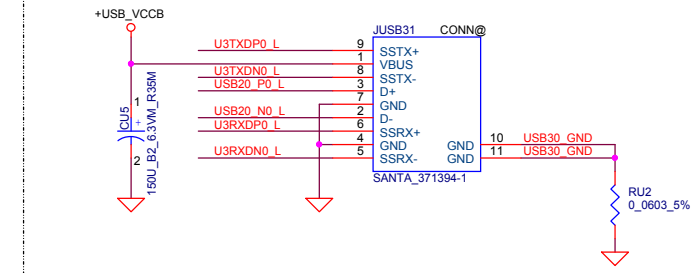


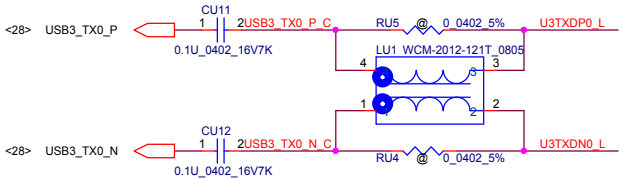


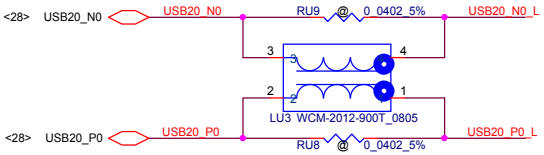


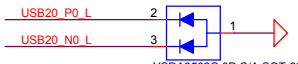


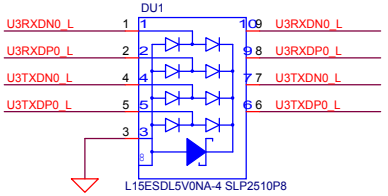




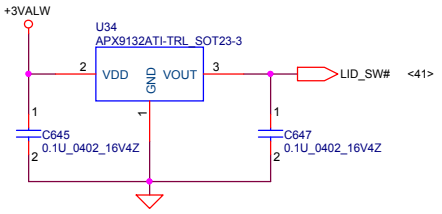




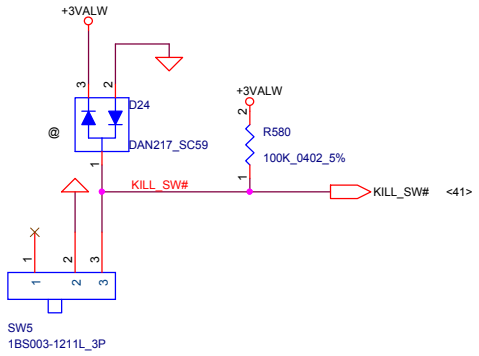




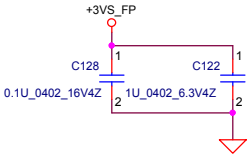
Lid SW

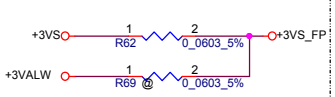


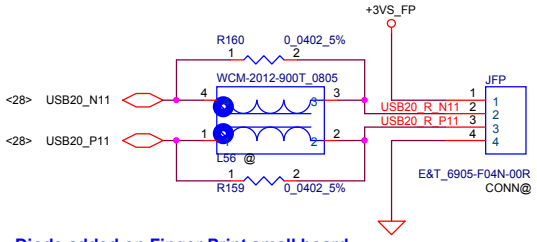
Kill Switch



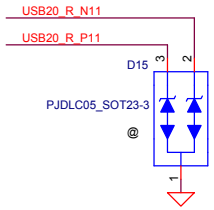
Finger Print



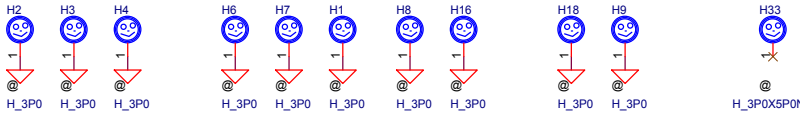




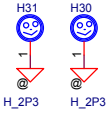
Diode added on Finger Print small board



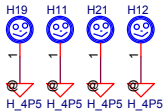
Screw Hole



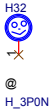
Break hole



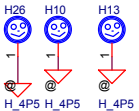
CPU



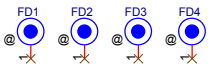
JWLAN

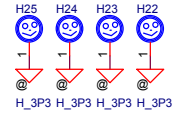


VGA



PCB Fiducial Mark PAD





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Issued Date	2011/09/23	Deciphered Date	2011/12/30

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Compal Electronics, Inc.

Title: KB/USB3.0/FP/LID/KW/PAD

Size | Document Number: QAQ10 LA-8581P M/B | Rev: 0.1

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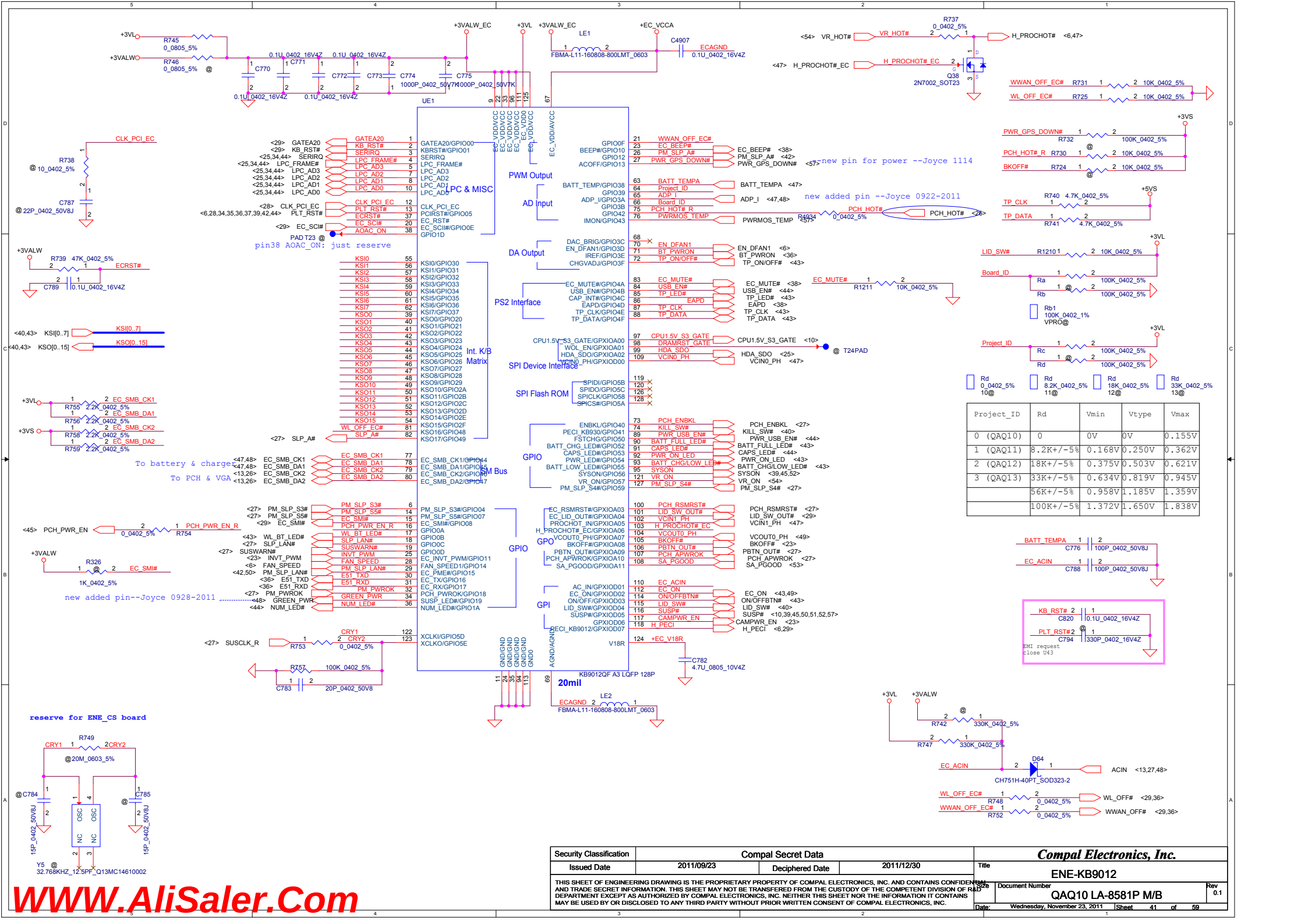

Project_ID	Rd	Vmin	Vtype	Vmax
0 (QAQ10)	0	0V	0V	0.155V
1 (QAQ11)	8.2K+/-5%	0.168V	0.250V	0.362V
2 (QAQ12)	18K+/-5%	0.375V	0.503V	0.621V
3 (QAQ13)	33K+/-5%	0.634V	0.819V	0.945V
	56K+/-5%	0.958V	1.185V	1.359V
	100K+/-5%	1.372V	1.650V	1.838V

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/09/23	Deciphered Date 2011/12/30	Title: ENE-KB9012

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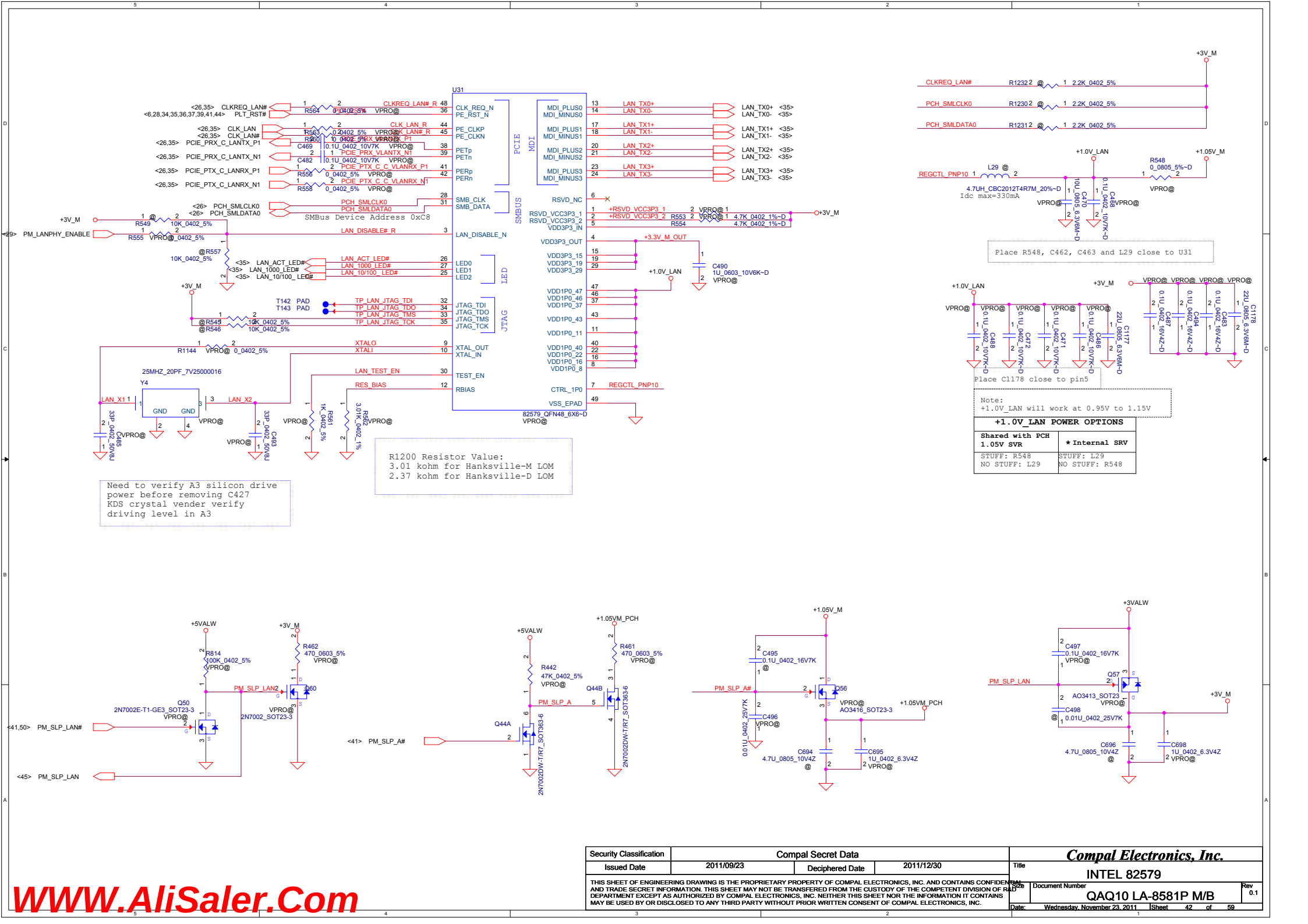
Size	Document Number: QAQ10 LA-8581P M/B		Rev: 0.1
Date: Wednesday, November 23, 2011	Sheet 41 of 59		



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Compal Electronics, Inc.	
Title	INTEL 82579
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Power Button/ PWR/B

TOP Side
Bottom Side

R152 @ 10K_0603_5%
R153 @ 10K_0603_5%
R154 100K_0402_5% @
R156 100K_0402_5%
+3VALW +3VL
D8 CHN202UPT SC-70
ON/OFFBTN# R
ON/OFFBTN# <41>
51_ON# <44,47>
<41,49> EC_ON
Q19 2N7002_SOT23-3 @
R155 10K_0402_5% @

JP7 ACES_51524-0080N-001 CONN@
PWR_ON_LED# +5VALW
ON/OFFBTN# R
KSO0 KSO0 <40,41>
KSI0 KSI0 <40,41>
KSI2 KSI2 <40,41>
KSI6 KSI6 <40,41>

Touch/B Connector

+5VS C755 0.1U_0402_16V4Z
JTP ACES_85201-0605N CONN@
TP_CLK <41>
TP_DATA <41>
LEFT_BTN#
RIGHT_BTN#
C757 @100P_0402_50V8J
C759 @100P_0402_50V8J

SW8 SMT1-05-A_4P LEFT_BTN#
SW7 SMT1-05-A_4P RIGHT_BTN#
TP_CLK TP_DATA LEFT_BTN# RIGHT_BTN#
D18 D16 PJDLC05C_SOT23-3
+3VS R214 10K_0402_5%
TP_ON/OFF# <41>
SW6 SMT1-05-A_4P

WL&BT LED

+3VS R210 10K_0402_5%
Q229A 2N7002DW-T/R7_SOT363-6
LED_WLAN# <36>
R1442 0_0402_5%
WL_BT_LED# <41>
+5VS R211 220_0402_5%
LED2 HT-191UYG5 0603 YELLOW GREEN
Q229B 2N7002DW-T/R7_SOT363-6

HDD LED

+3VS R199 10K_0402_5%
Q210A 2N7002DW-T/R7_SOT363-6
MEDIA_LED#
+5VS R200 220_0402_5%
LED4 HT-191USD 0603 RED
Q210B 2N7002DW-T/R7_SOT363-6

BATT CHARGE/FULL LED

Vf=2.1V(typ),2.4V(max) for amber
Vf=2.2V(typ),2.4V(max) for green
If=25mA(max)

+5VALW LED5 HT-297USD/UYG 0603 RED/YELLOW GREE
R203 220_0402_5% BATT_CHG/LOW_LED# <41>
R204 220_0402_5% BATT_FULL_LED# <41>
<41> 5IN1_LED#
<25> SATA_LED#
+3VS Q230A 2N7002DW-T/R7_SOT363-6 3Q230B
MEDIA_LED#
R85 0_0402_5%

PWR ON LED

+5VALW LED6 HT-191UYG5 0603 YELLOW GREEN
R202 220_0402_5%
Q6 2N7002_SOT23-3
PWR_ON_LED# PWR_ON_LED <41>

+5VS R215 220_0402_5% LED8 LED 19-213A/T1D-CP2Q2HY/3T 0603 WHITE
TP_LED# <41>

Left USB

+USB_VCCB W=40mils
C2 220U_6.3V_M
C7 0.1U_0402_16V4Z
C8 1000P_0402_50V7K

<28> USB20_N1
<28> USB20_P1
R1 0_0402_5%
L3 WCM-2012-900T_0805
R5 0_0402_5%
USB20_N1_R
USB20_P1_R
@D11 PJDLC05_SOT23-3
JUSB1 SANTA_360117-1 CONN@

+5VALW C3 0.1U_0402_16V4Z
+USB_VCCE W=80mils
U6 RT9715BGS_SO8
<6,11,40,45> SUSP
<40,45> SYSON#
R9 0_0402_5%
R10 @ 0_0402_5%
R4 0_0402_5%
USB_OC4# <28,40>
C12 @ 0.1U_0402_16V4Z
C4 4.7U_0805_10V4Z
C14 0.1U_0402_16V4Z

D13 PJDLC05_SOT23-3 @

ESATA

+USB_VCCB W=40mils
C9 220U_6.3V_M @
C10 0.1U_0402_16V4Z
C11 1000P_0402_50V7K

<28> USB20_N9
<28> USB20_P9
R163 0_0402_5%
L57 WCM-2012-900T_0805
R162 0_0402_5%
USB20_N9_R
USB20_P9_R

<25> SATA_PTX_DRX_P4
<25> SATA_PTX_DRX_N4
<25> SATA_PRX_C_DTX_N4
<25> SATA_PRX_C_DTX_P4
C2055 0.01U_0402_25V7K SATA_PTX_C_DRX_P4
C2054 0.01U_0402_25V7K SATA_PTX_C_DRX_N4
C2052 0.01U_0402_25V7K SATA_PRX_DTX_N4
C2053 0.01U_0402_25V7K SATA_PRX_DTX_P4

JESATA FOX_3Q318111-R33C3-7F CONN@

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Compal Electronics, Inc.

Title: PWR/TP/LED
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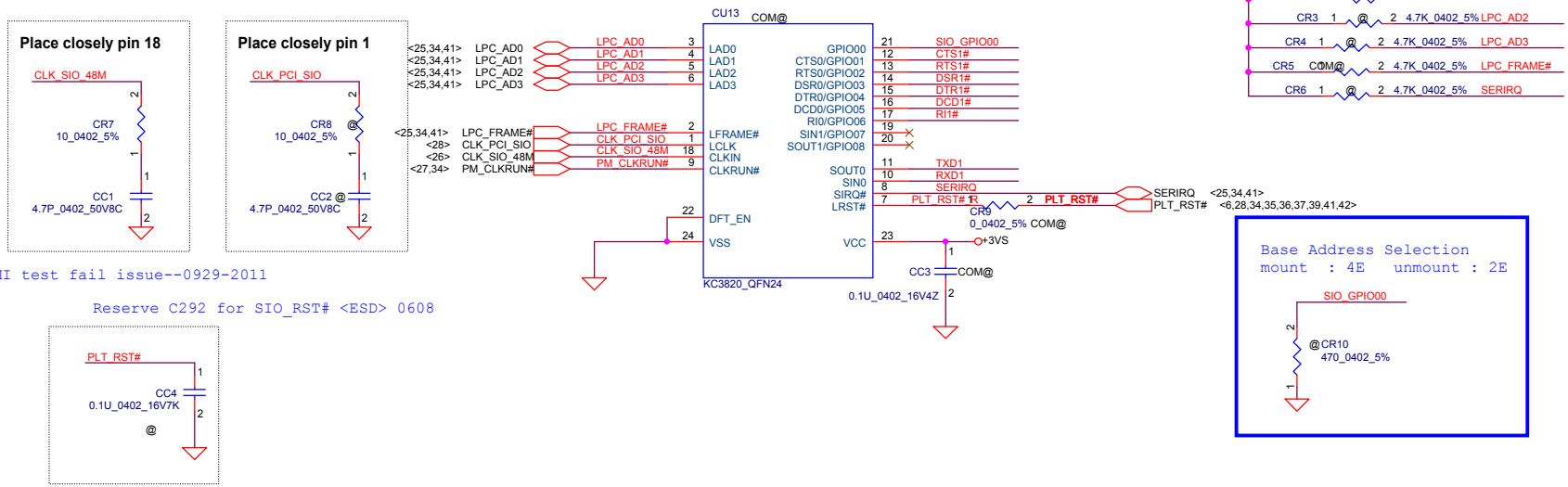
EMI And ESD

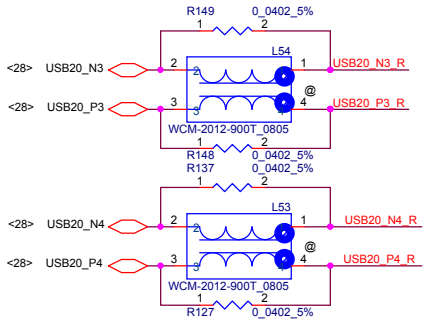
Reserve R199,C207,R226,C208 <EMI> 0601

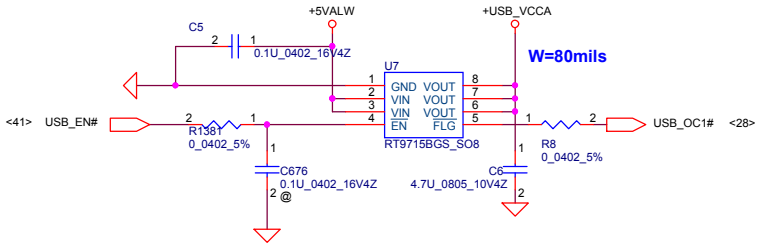


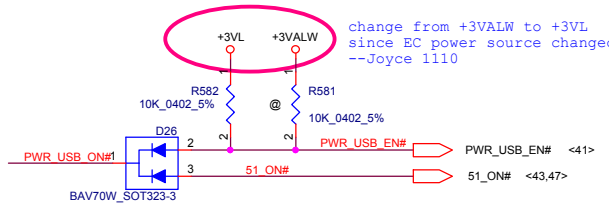
Add CR7,CC1 for EMI test fail issue--0929-2011

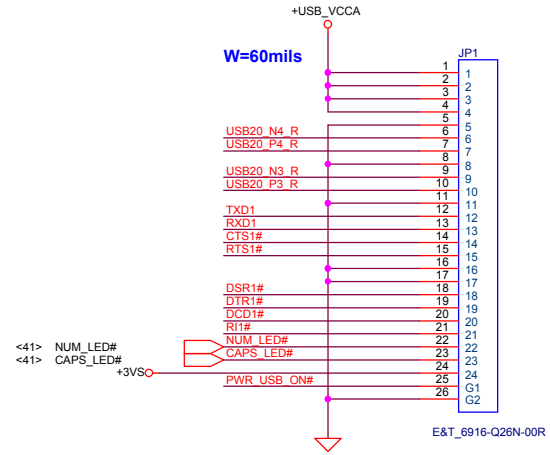
Reserve C292 for SIO_RST# <ESD> 0608

PWR USB









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Compal Electronics, Inc.

Title: POWER USB / COM

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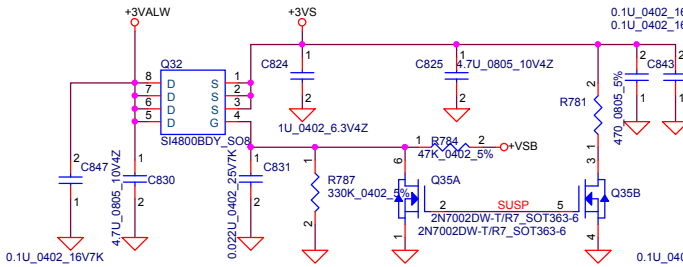
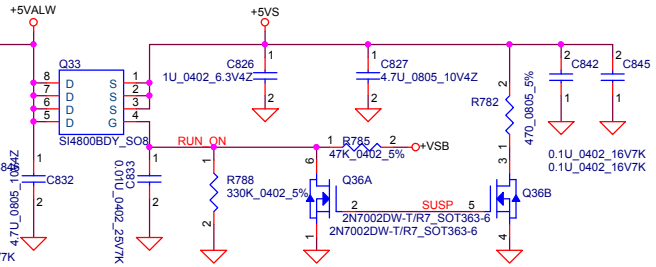
+3VALW TO +3VS

Vgs=-0V,Id=9A,Rds=18.5mohm

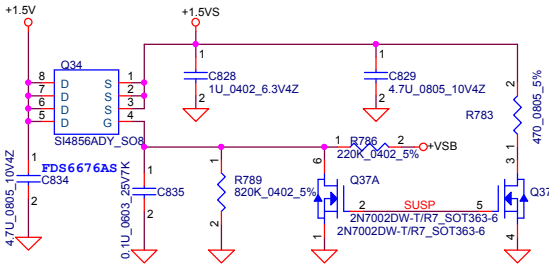


+5VALW TO +5VS

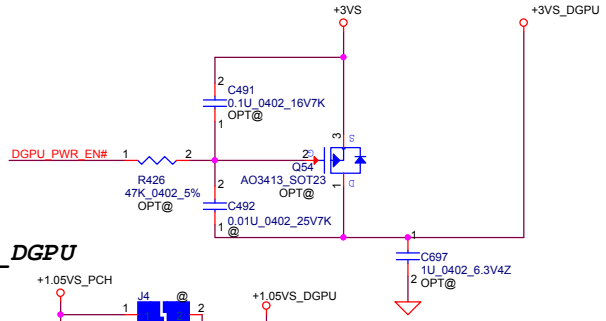


+1.5V to +1.5VS

Vgs=10V,Id=14.5A,Rds=6mohm

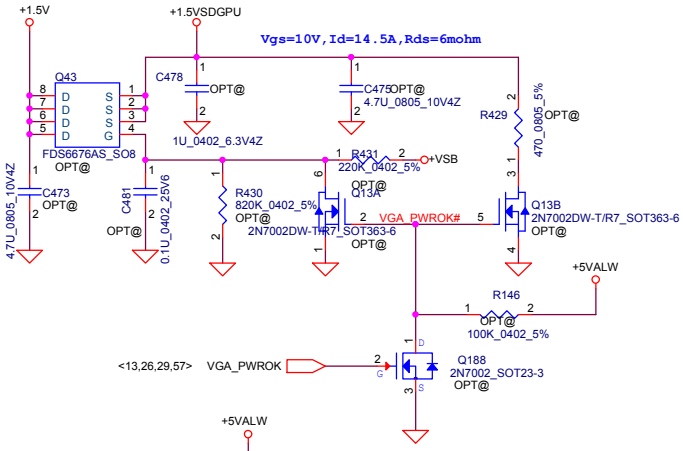


+3VS to +3VS_DGPU



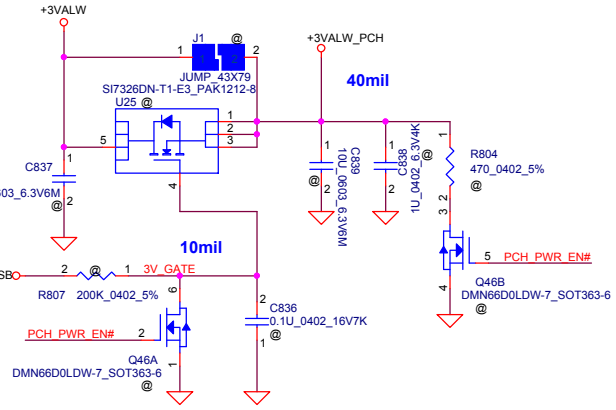
+1.5V to +1.5VSDGPU

Vgs=10V,Id=14.5A,Rds=6mohm

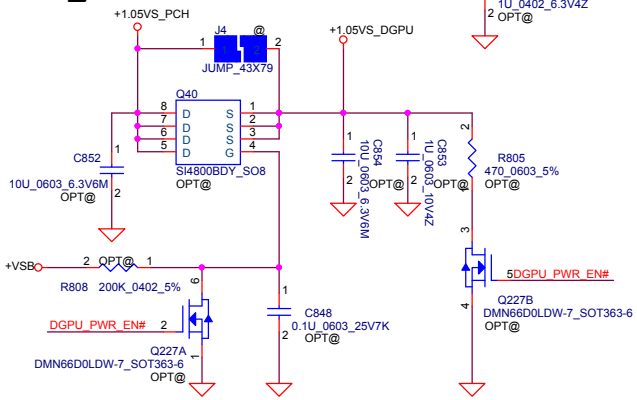


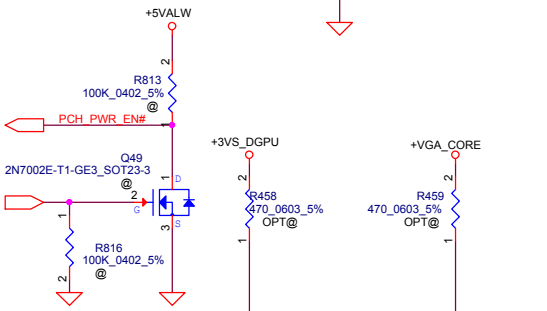
+3VALW TO +3VALW(PCH AUX Power)

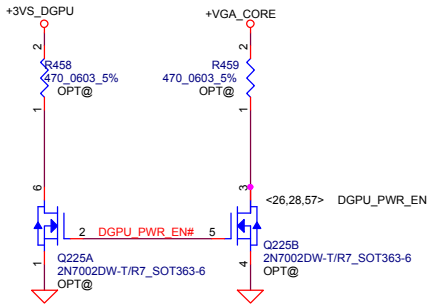
Short J1 for PCH VCCSUS3.3

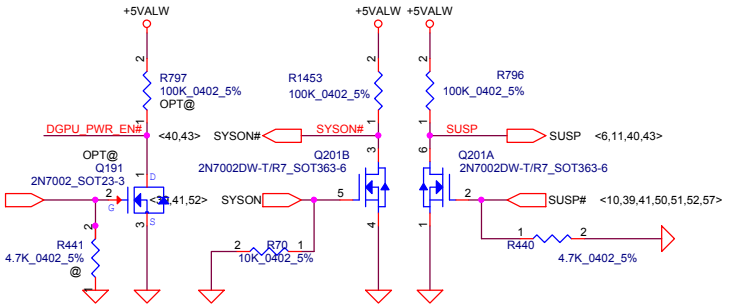


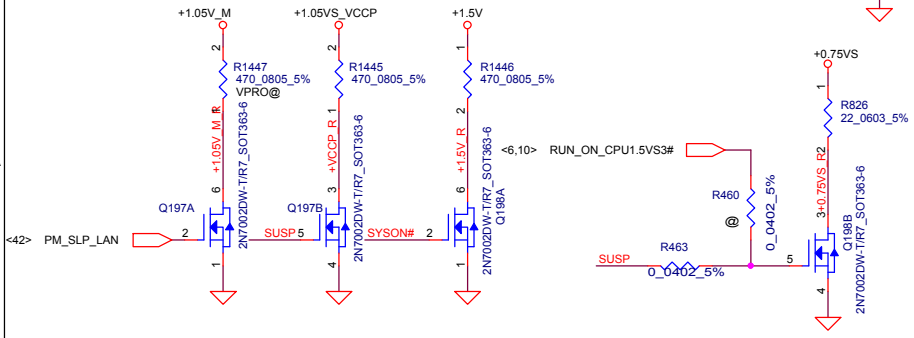
+1.05VS_DGPU











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Compal Electronics, Inc.

Title: DC-DC INTERFACE

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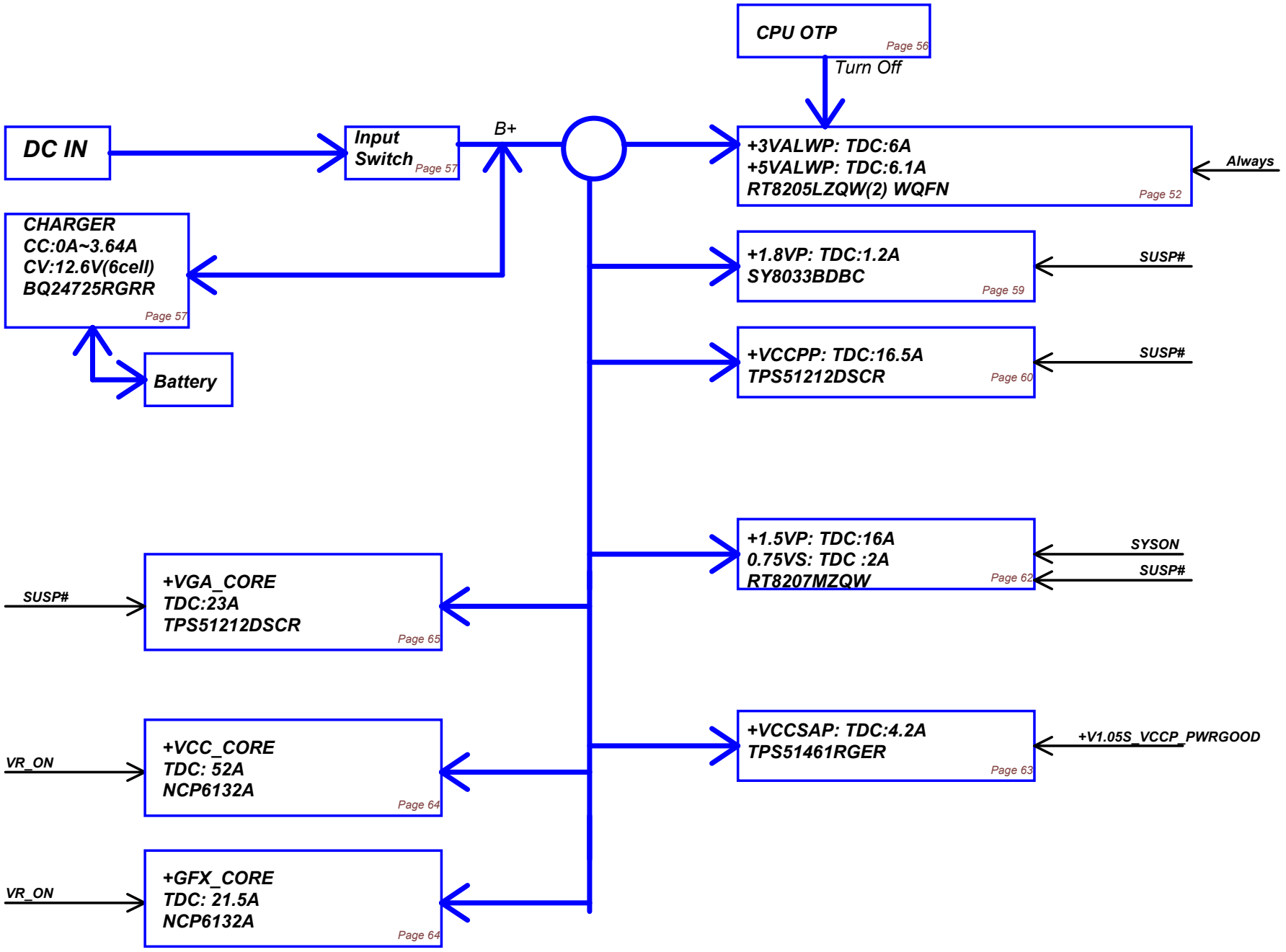
Power block



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Compal Electronics, Inc.

Title: POWER BLOCK DIAGRAM

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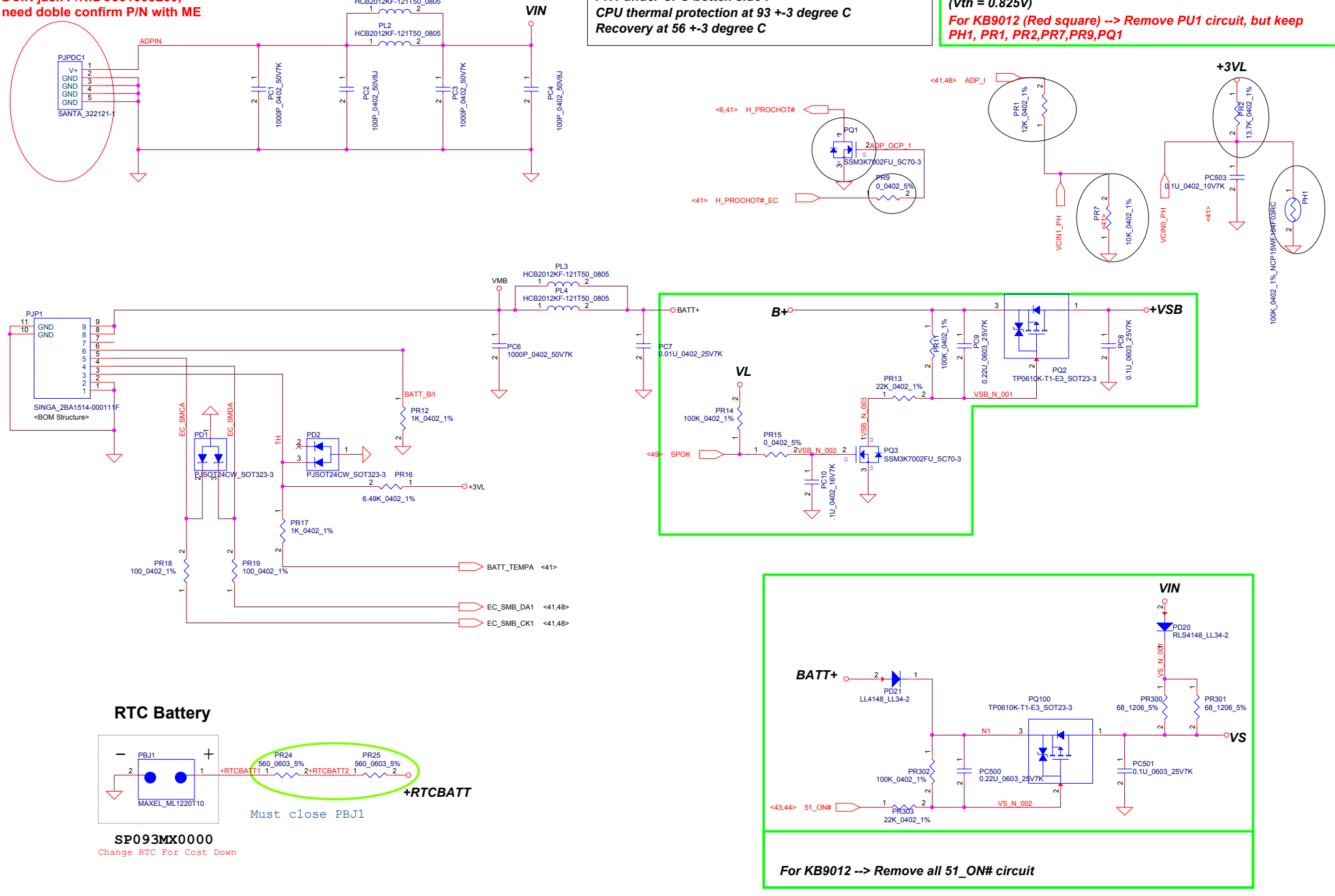
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep
PH1, PR1, PR2,PR7,PR9,PQ1



For KB9012 --> Remove all 51_ON# circuit

RTC Battery

Must close PBJ1

SP093MX0000
Change RTC For Cost Down

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Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

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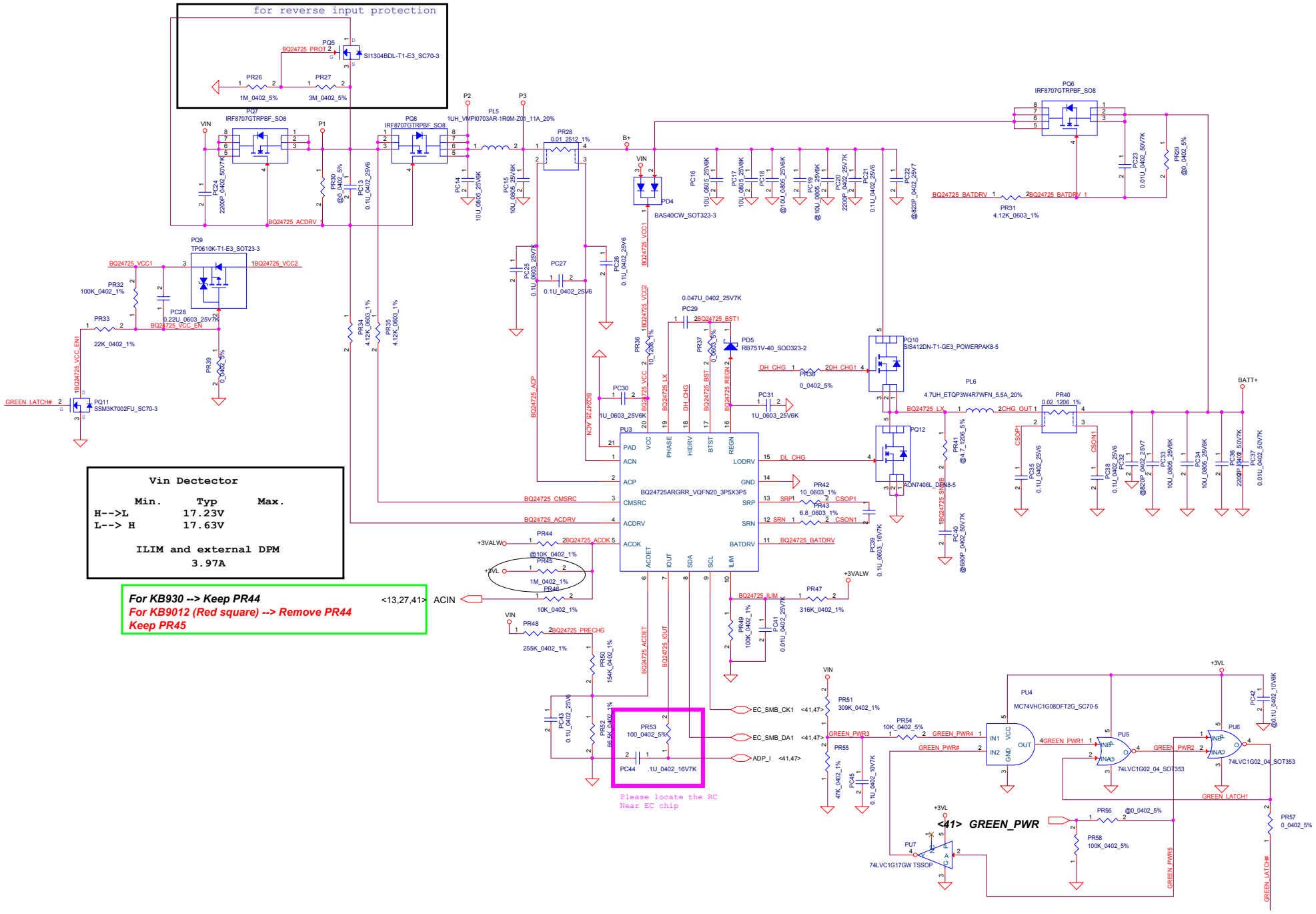

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Title	PWR-CHARGER
Size	Document Number: QAQ10, LA-8581P MB
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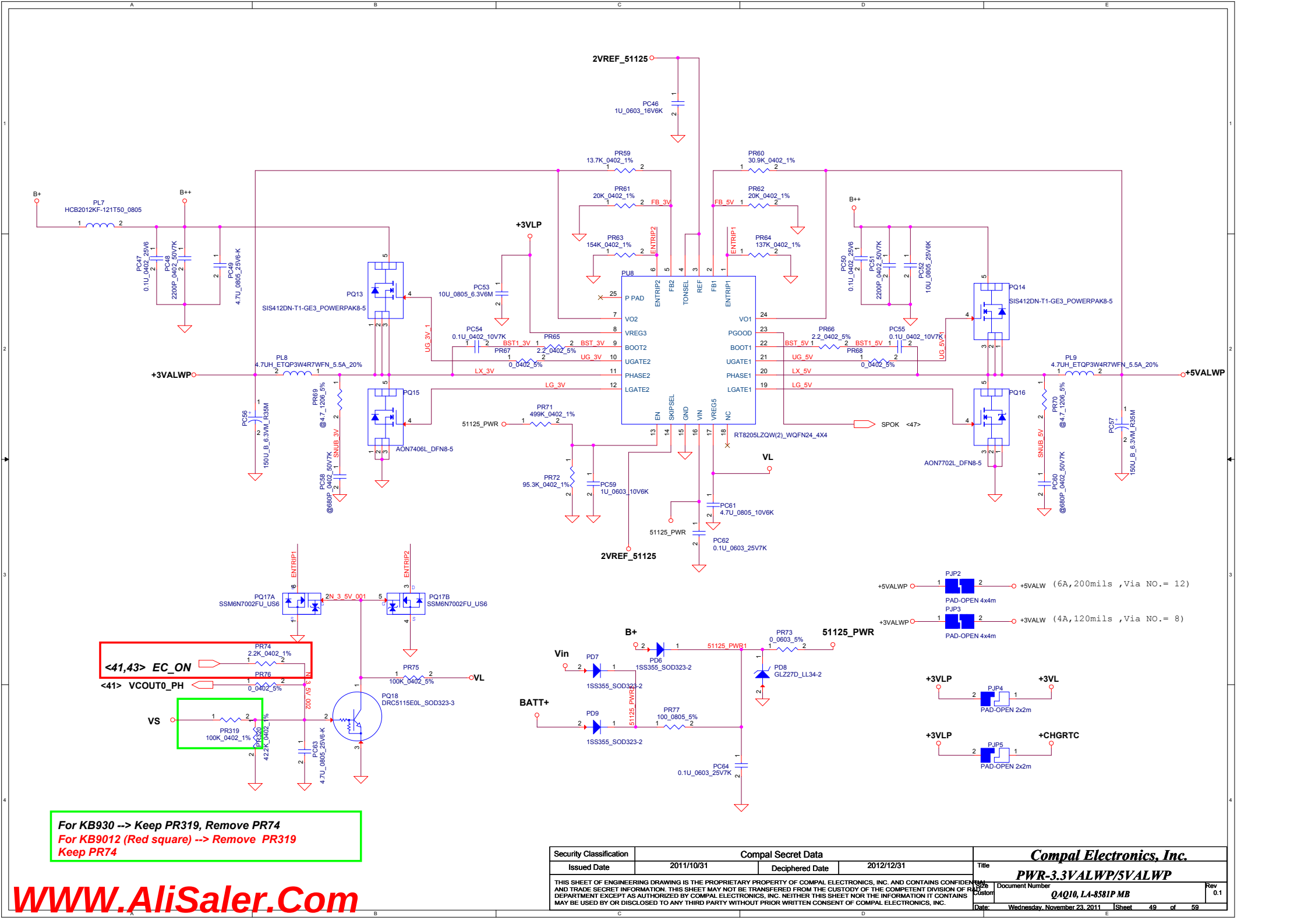

For KB930 --> Keep PR319, Remove PR74
For KB9012 (Red square) --> Remove PR319
Keep PR74

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Compal Electronics, Inc.

Title: **PWR-3.3VALWP/5VALWP**

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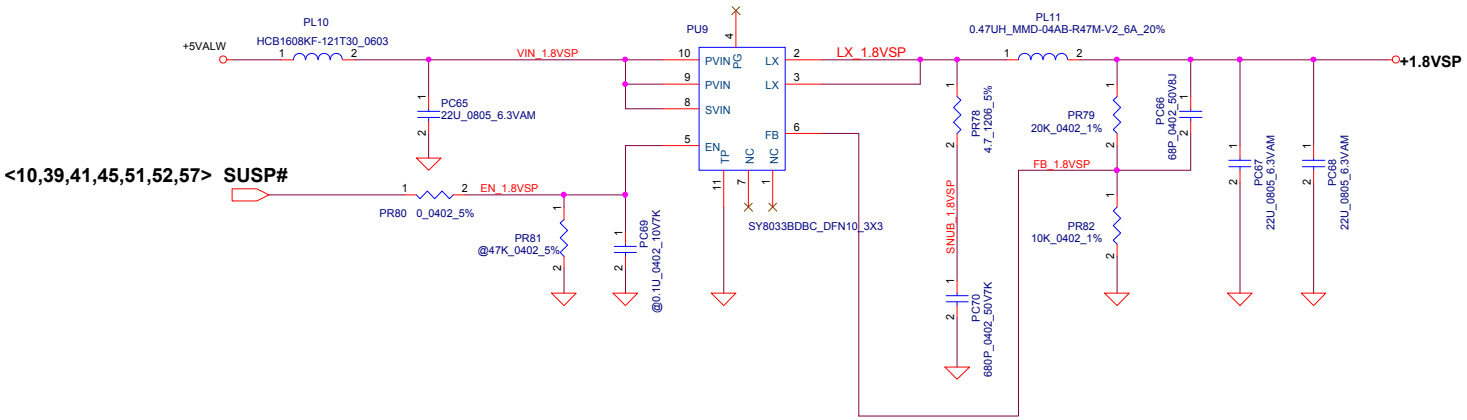

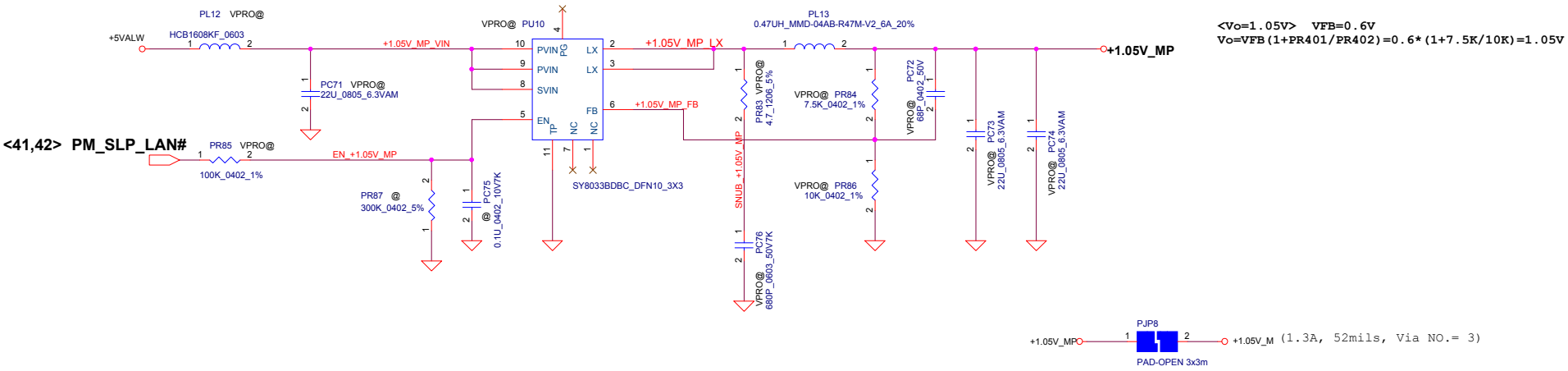

<Vo=1.05V> VFB=0.6V
Vo=VFB(1+PR401/PR402)=0.6*(1+7.5K/10K)=1.05V

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Compal Electronics, Inc.

Title: PWR-1.8VSP,1.05V_MP

Size | Document Number: QAQ10, LA-8581P MB | Rev: 0.1

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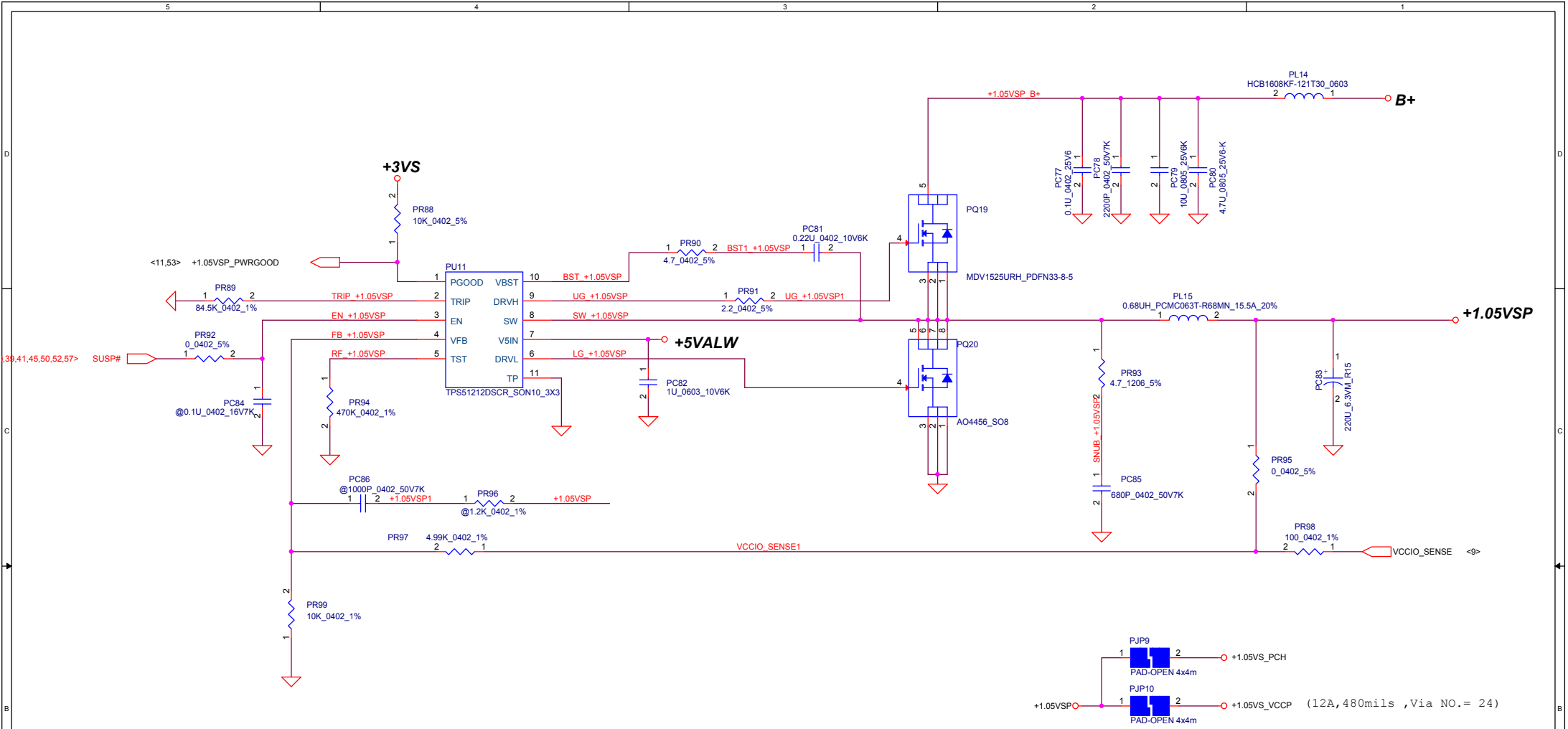

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Issued Date	2011/10/31	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: PWR-+1.05VSP

Size	Document Number	Rev
Custom	QAQ10, LA-8581P MB	0.1

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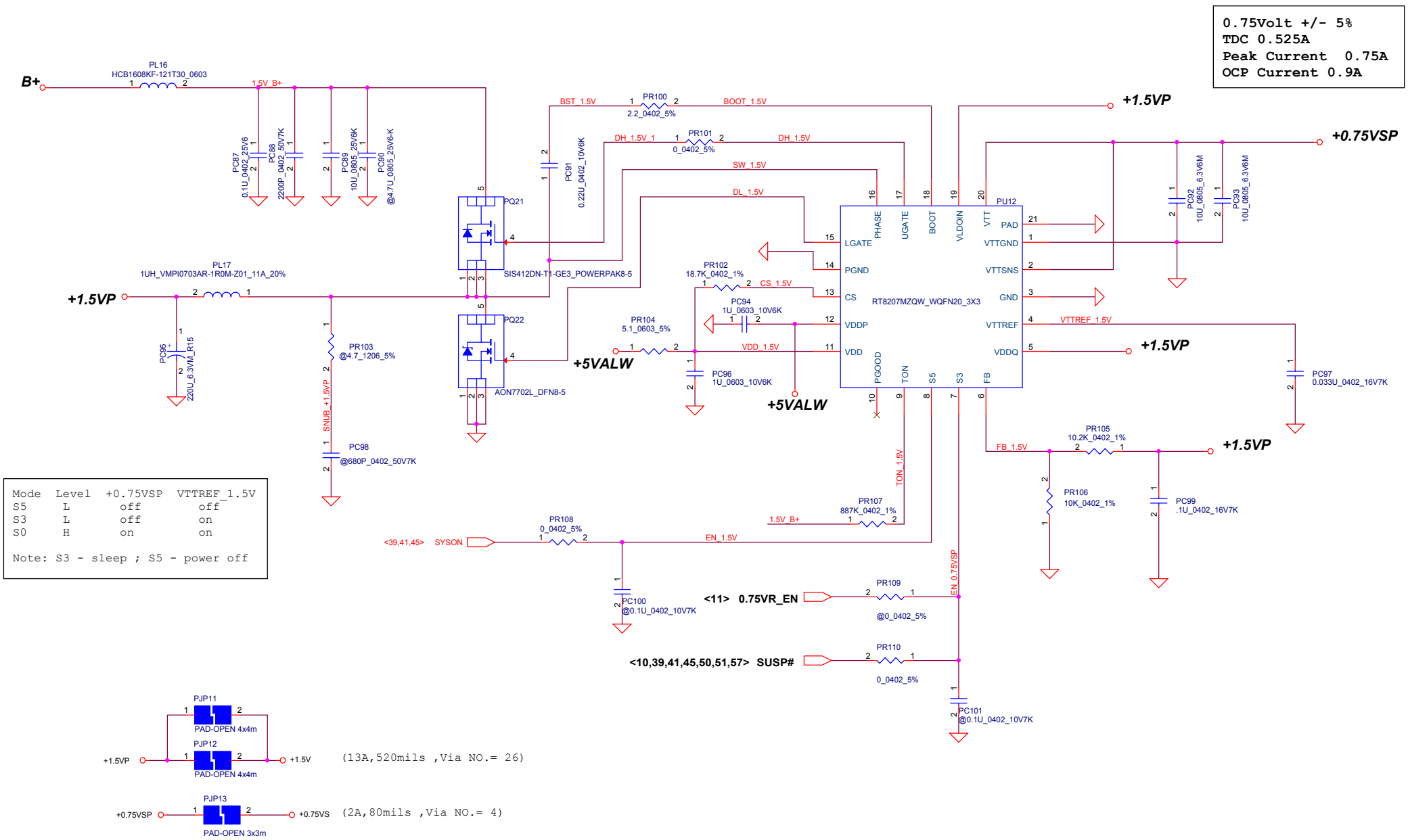

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Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

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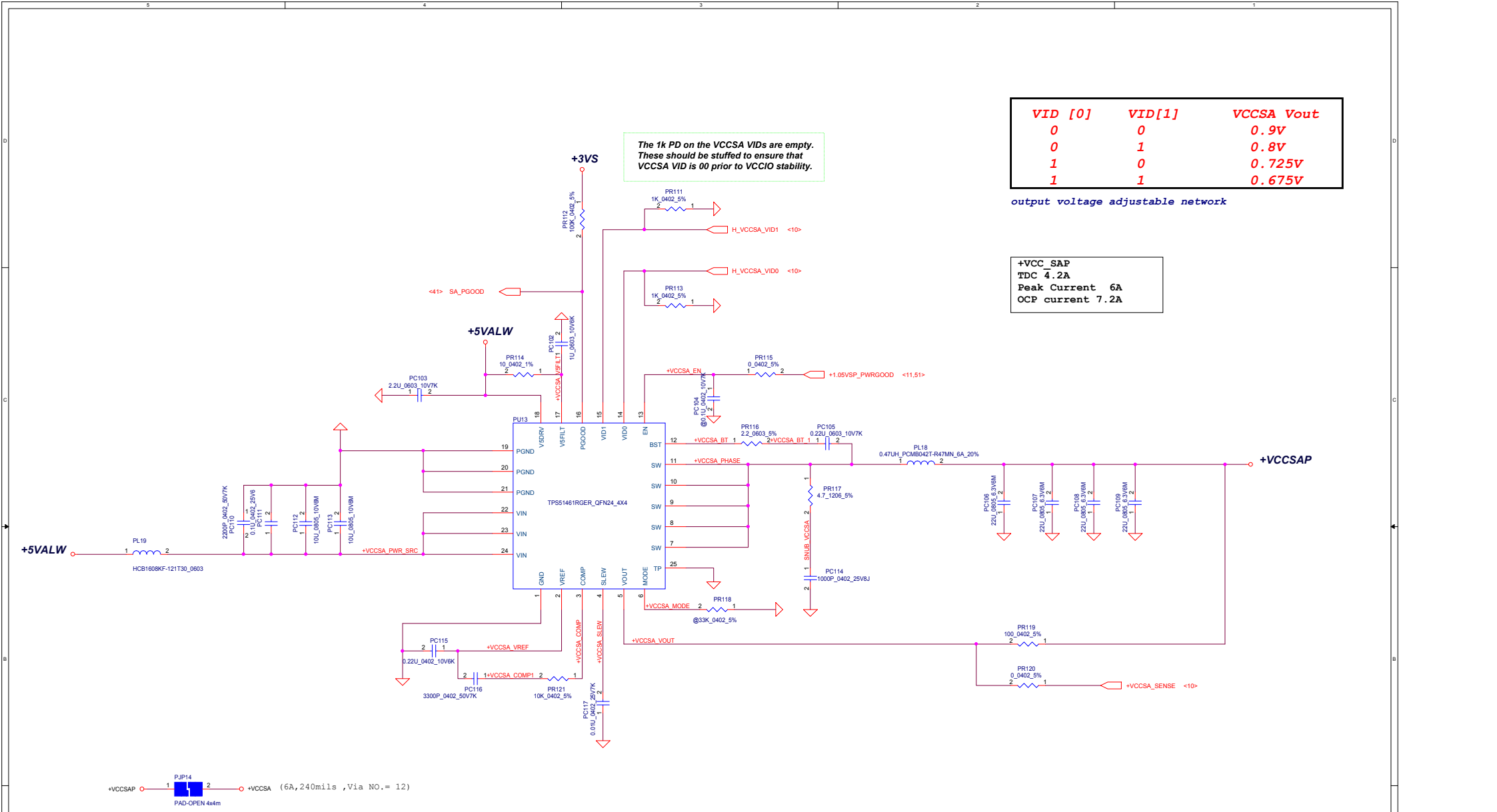
VID [0] VID[1] VCCSA Vout
0 0 0.9V
0 1 0.8V
1 0 0.725V
1 1 0.675V
output voltage adjustable network
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
+3VS
+5VALW
+VCCSAP
PU13
TPS51461RGER_QFN24_4X4
PL19
HCB1608KF-121T30_0603
PL18
0.47UH_PCMB042T-R47MN_6A_20%
PJP14
PAD-OPEN 4x4m
+VCCSAP (6A,240mils ,Via NO.= 12) +VCCSA
H_VCCSA_VID1 <10>
H_VCCSA_VID0 <10>
<41> SA_PGOOD
+1.05VSP_PWRGOOD <11,51>
+VCCSA_SENSE <10>
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Compal Electronics, Inc.
PWR-VCCSAP
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CSP1A, CSP2A to +5VS.

LGA, SWA, HGA, BSTA, DIFFA, TRBSTA#, ILIMA, PWMA are float.

VSPA, VSNA to GND (HW side). FBA and COMPA are short.

CSREFA, TSNSA, IOUTA to GND. CSCOMPA, CSSUMA, DROOPA are short.

DIS only:
All AXG components are @.
Except
PR272 and PR273 are 0ohm.
PC223, PC226, PR202 are 0ohm.
PC220, PC215, PR206 are 0ohm.

PUT COLSE TO GT Inductor

PUT COLSE TO V_GT HOT SPOT

PUT COLSE TO VCORE HOT SPOT

PUT COLSE TO VCORE Phase 1 Inductor

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Title: PWR-CPU_CORE

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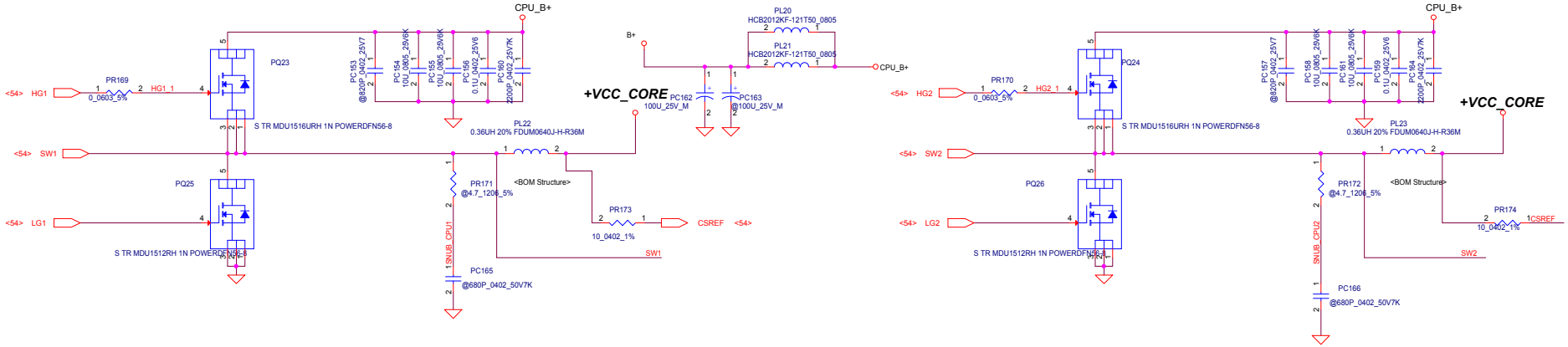

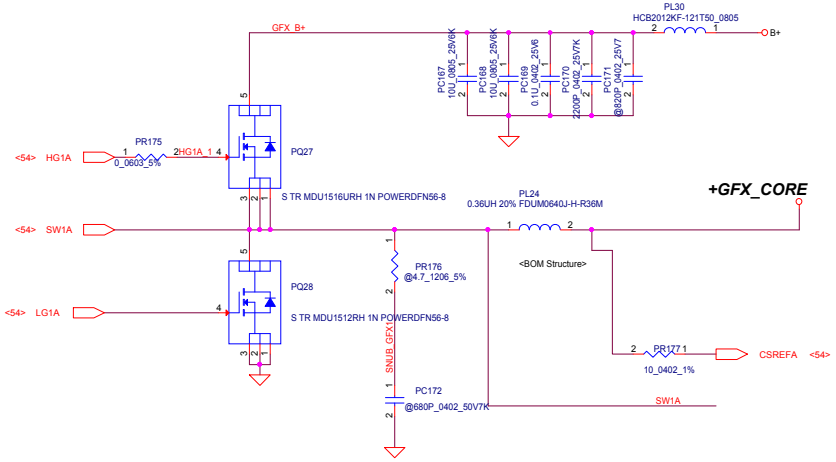

QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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Title: ***PWR-VCC_CORE***

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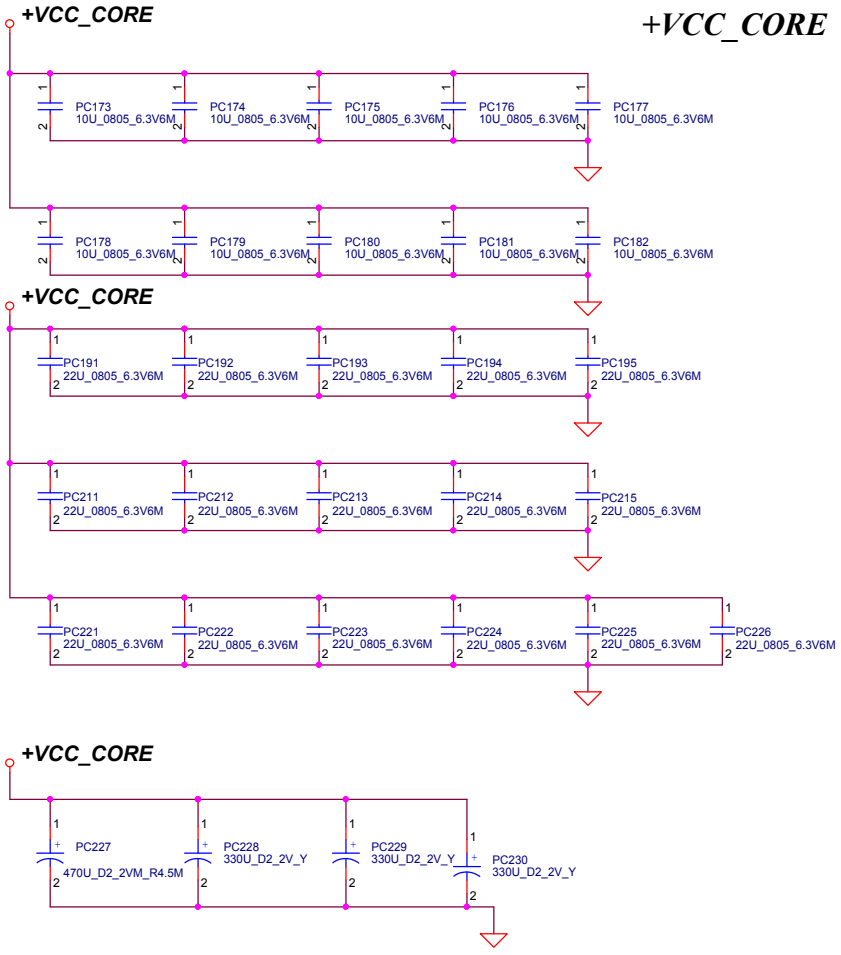
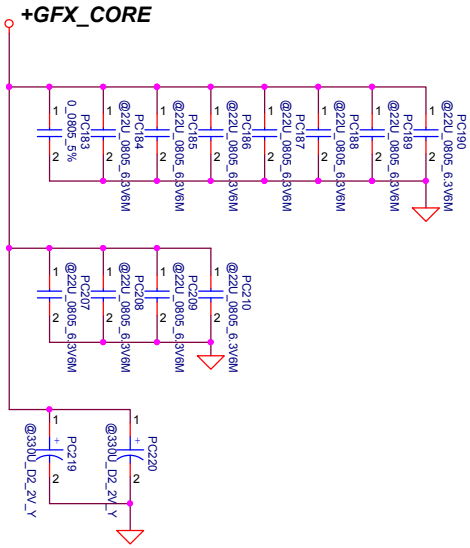


+VCC_CORE

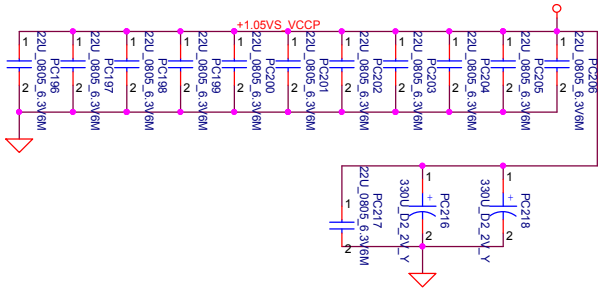
+GFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+1.05VS_VCCP



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Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

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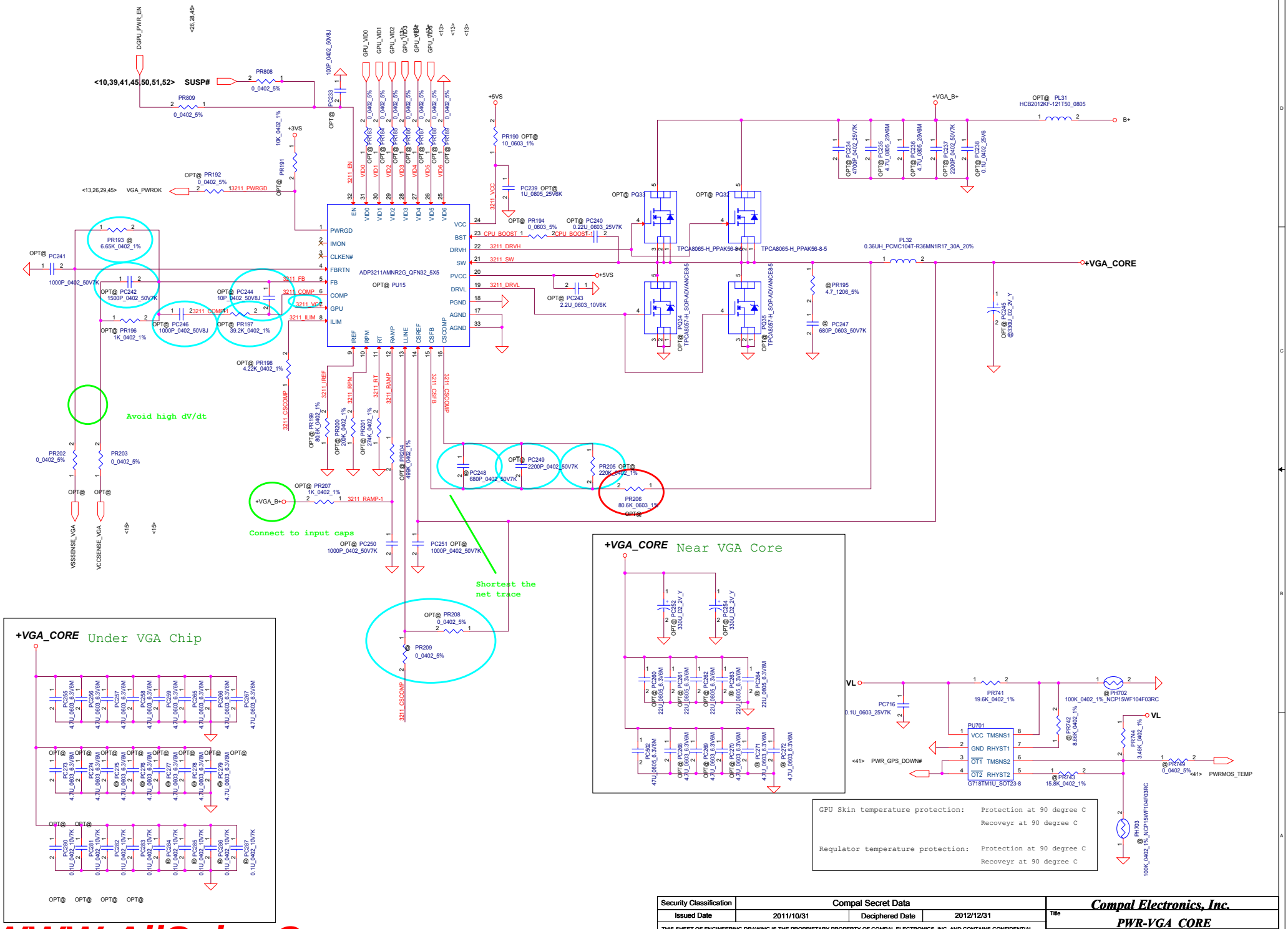

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Compal Electronics, Inc.			
Title: PWR-VGA_CORE			
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